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# Study of a triggered, full event zero-suppressed front-end readout chain operating up to 1 MHz trigger rate and 300 pile-up for CMS Outer Tracker upgrade at HL-LHC

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## *Front-End readout chain for CMS Outer Tracker*

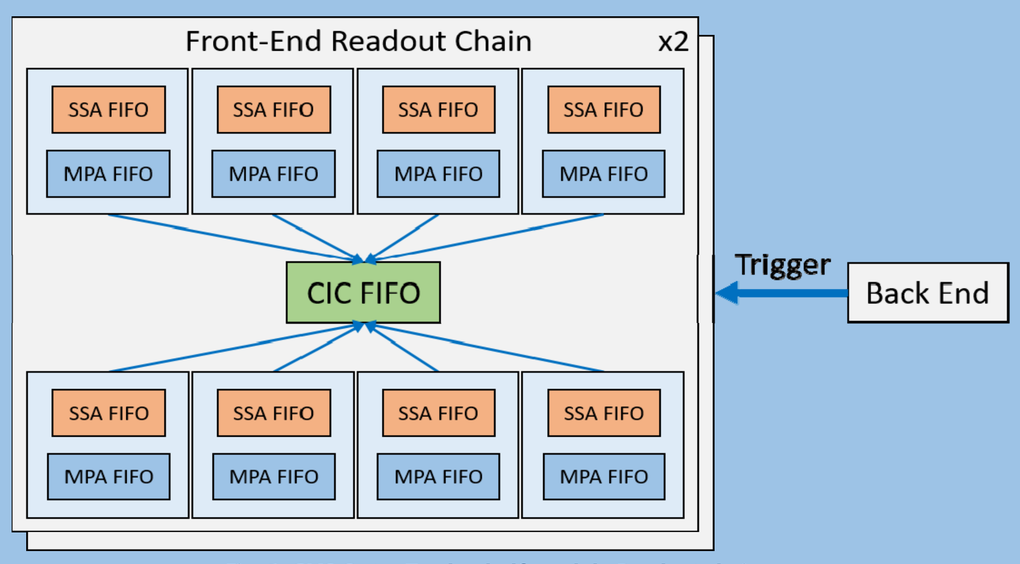



*Fig. 1: CMS Outer Tracker half-module Readout chain*

The CMS Outer Tracker readout electronics [1] at the HL-LHC [2] will have to cope with **300 Pile-Up (PU) events** per bunch crossing for the inner modules, closer to the collision point.
An efficient event selection needs an increased **trigger rate of 750 kHz** and a **latency of 12.8 $\mu s$**, larger than the ones used in the existing system, to readout the full event.
The large event size of 32 Gbps does not fit the limited output bandwidth per module of 1.28 Gbps. Therefore, upon the reception of a Trigger from the Back-End, **32 sensor readout ASICs** (16 SSA [3], 16 MPA [4]), provide the zero-suppressed full event to **2 data concentrator ASICs** (CIC [5]).
The limited output data bandwidth and the random value of trigger arrival times makes necessary a **temporary on-chip data storage**.

This study aims at presenting the methodology followed during the development and implementation of a **multichip FIFO-based architecture** for a **low-power** density less then 100 $mW/cm^2$ featuring a **robust event synchronization** among chips. To accurately size FIFOs, a multichip simulation based on physics Monte Carlo samples has been performed.

The architecture should show an event loss due to **buffer inefficiencies below $10^{-6}$** with a PU of 300 and a trigger rate of 1 MHz in the inner layer of the Outer Tracker of CMS experiment.

## *ASICs triggered readout architecture*

***All the FIFO employed in this multichip system are based on latches and pointers to save power.***

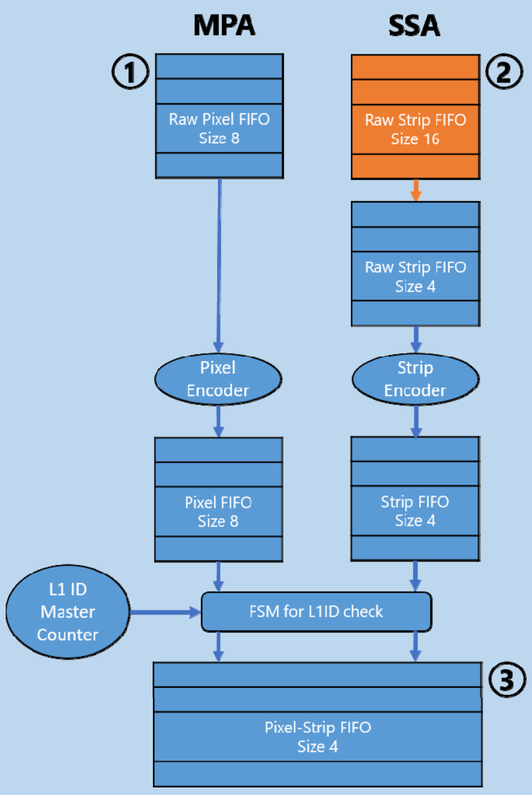



*Fig. 2: FIFO-based architecture of the FE ASICs*

**SSA:** Each SSA ASIC needs to store on a FIFO several events before sending out to the corresponding MPA a fixed size, no zero-suppressed packet containing the full strip event.

**MPA:** Each MPA ASIC has to store on a FIFO, called Raw Pixel FIFO, the full pixel event, while storing the full strip event by the corresponding SSA ASIC in another FIFO, called Raw Strip FIFO.
Pixel encoding and strip encoding are needed to reduce the output bandwidth creating a zero-suppressed full event that will have a variable size depending on the pile-up condition.
Two more FIFOs, one for pixels and another for strips are inserted before the L1 FIFO where the information from strip layer and pixel layer are combined together.

**CIC:** 2 Data Concentrator ASICs, called Concentrator Integrated Circuit (CIC), are necessary to readout 16 ASICs each. In particular, a CIC, receives raw data from 8 MPA/SSA pairs.
Therefore, a total number of 8 FIFOs has been implemented to store Pixel-Strip zero-suppressed and variable size packet events.

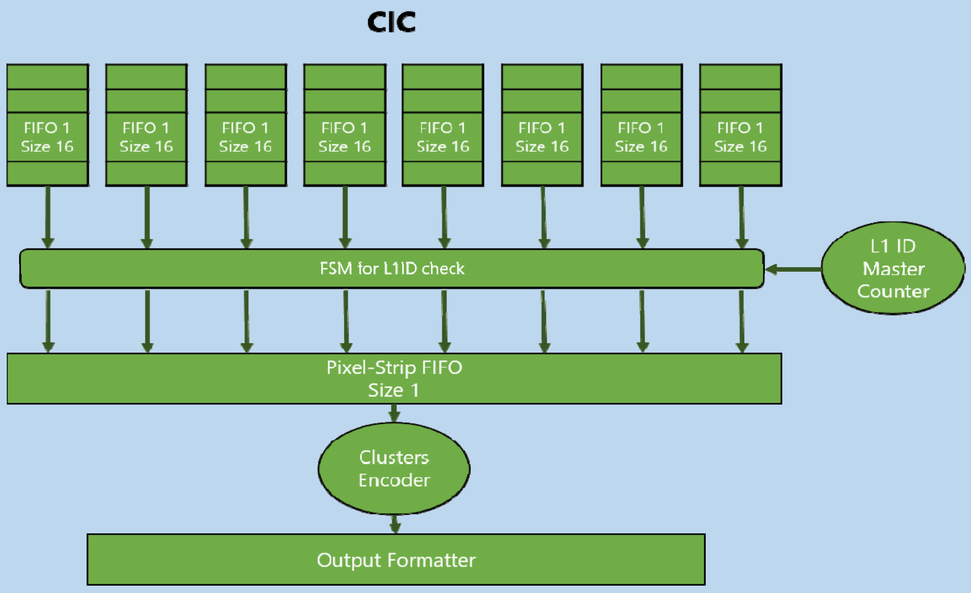



*Fig. 3: FIFO-based architecture of the Data Concentrator ASIC*

**Event Synchronization:**
In both architectures a Finite State Machine (FSM) has been implemented to allow robust synchronization among ASICs. It allows comparing the L1 ID used to tag the event packets and an ideal L1 ID, called Master L1 ID. This check is done internally in the ASICs and is fundamental to handle exceptions without losing synchronization among ASICs in the multichip system.
In particular, the L1 ID Master is provided by a counter that emulates the behavior of a FIFO counting the number of Triggers received. The choice of employing a counter is the safest in terms of reliability because it allows a full triplication and voting, overcoming any problem that could unluckely come from a Single-Event Upset (SEU). In addition, the counter would roll over and there is no condition of full FIFO in this kind of implementation.

## Buffer (FIFO) sizing and inefficiency studies

As explained in reference [6], the queueing inefficiencies in the system are determined by the ratio between input and output rates and the queue (or FIFO length). This relation is shown in Figure 4.
For different I/O rate, a specific FIFO length needs to be implemented to have buffer inefficiencies less than a desired value. The ratios are different for every FIFO.

With reference to Figure 2:
**Case 1 - Encoder buffer:** Input rate is the L1 rate, approximated to 1 MHz, while the output rate is represented by the speed of the encoder, approximated to a worst case of 2 clock cycles fixed plus 3 particle encoded per cycle. At PU 300, we expect an average of 4 particle per MPA that leads to a ratio of 0.35. A buffer length of 16 is needed to keep inefficiencies below $10^{-6}$.

**Case 2 - Fixed length data transmission buffer:** Input rate is the L1 rate, approximated to 1 MHz, while the output rate is represented by the speed of the data packet transmission, in this specific case is 23 clock cycles. The ratio is approximated to 0.6 which requires a buffer length of 16 events to keep the inefficiency below the limit of $10^{-6}$.

**Case 3 - Variable length data transmission buffer:** Input rate is represented by the data packet to be transmitted, in this case of 31 bits per particle with an header of 42 bits and a dead-time between consecutive events of 5 cycles (worst case), while the output rate is determined by the speed of the output datalink, in this case 320 Mbps. Assuming to be in the worst case scenario at 300 PU, the calculated ratio is approximated to 0.65 which requires a buffer depth of 16 events. However, in this case we can also profit from the previous buffers that would store the events in case the last FIFO is full.

**Buffer inefficiency**

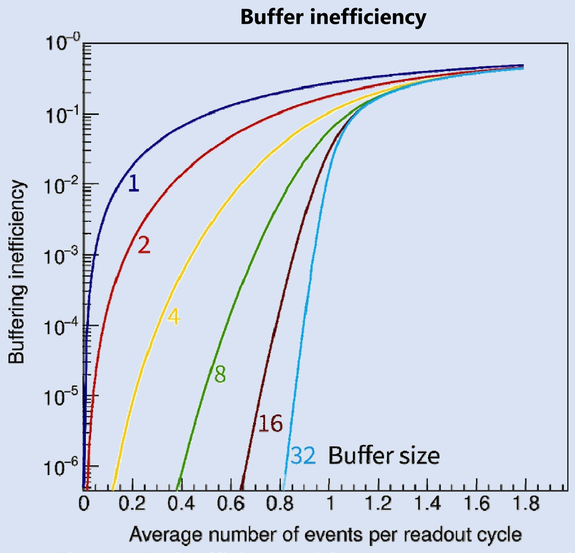
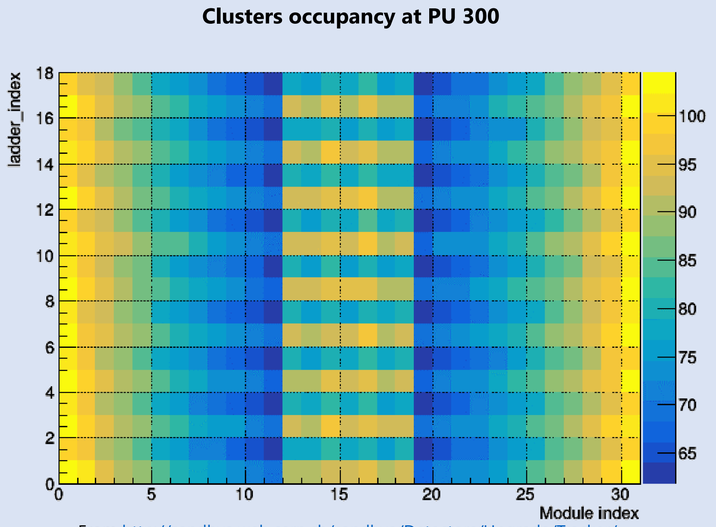



*Fig. 4: FIFO inefficiency with respect to I/O rate ratio*

**Clusters occupancy at PU 300**




From http://sandhya.web.cern.ch/sandhya/Detectors/Upgrade/Tracker/

*Fig. 5: Cluster Occupancy in the inner barrel layer*

The method explained, provided the buffer sizing shown in Figure 2 and 3, should limit **the buffer losses below $10^{-6}$**.
The main limitation to finalize the study is the simulation runtime, that is in the order of 1 s of real-time = 1 µs of simulation. It is important to have an analytical approach, but also proving it trough simulation.
The analytical studies presented above have been followed by extensive simulations with UVM-based testbench framework [7], to prove the robustness of the system: no buffer inefficiency observed in 25 ms at PU 300 and 1 MHz input rate which provides a buffer inefficiency below $5x10^{-5}$.

***References:***
[1] A. H. Dierlamm, *The CMS Outer Tracker for HL-LHC, 2018 CMS-CR-2018-014.*
[2] CMS collaboration, *Technical proposal for the Phase-II upgrade of the Compact Muon Solenoid*, CERN-LHCC-2015-010, LHCC-P-008 (2015).
[3] A. Caratelli, Y. Leblebici, J. Kaplon, D. Ceresa, J. Murdzek, K. Kloukinas and S. Scarfì, *Short-Strip ASIC (SSA): A 65nm silicon-strip readout ASIC for the Pixel-Strip (PS) module of the CMS Outer Tracker detector upgrade at HL-LHC*, PoS. (2018): 031.
[4] D. Ceresa, J. Murdzek, K. Kloukinas, J. Kaplon, A. Caratelli and S. Scarfì, *Design and simulation of a 65 nm Macro-Pixel Readout ASIC (MPA) for the Pixel-Strip (PS) module of the CMS Outer Tracker detector at the HL-LHC*, PoS. (2018): 032.
[5] B. Nodari, L. Caponetto, G. Galbit, S. Scarfì and S. Viret, *A 65 nm Data Concentration ASIC for the CMS Outer Tracker Detector Upgrade at HL-LHC,* In *Topical Workshop on Electronics for Particle Physics (TWEPP2018)*, vol. 17, p. 21. 2018.
[6] Øveräs H., *Dead-time losses in a buffered data recording system*, Nuclear Instruments and Methods 1972 Oct 1;104(1):85-91.
[7] S. Scarfì, A. Caratelli, D. Ceresa, K. Kloukinas, Y. Leblebici, L. Caponetto, G. Galbit, B. Nodari and S. Viret, *A System-Verilog Verification Environment for the CIC Data Concentrator ASIC of the CMS Outer Tracker Phase-2 Upgrades*. No. CMS-CR-2018-282. 2018.

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