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Study of a triggered, full event zero-suppressed front-end readout chain operating up to 1 MHz trigger rate and 300 pile-up for CMS Outer Tracker upgrade at HL-LHC

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The CMS Outer Tracker at HL-LHC will have to cope with 300 pile-up events per bunch crossing and to improved tracking performance while operating at a trigger rate up to 1 MHz. The front-end electronics readout chain consists of sensor readout ASICs connected to a data concentrator ASIC featuring zero-suppression. This contribution presents the methodology and the analysis work for the sizing of a multichip FIFO-based architecture and implementation of a full exception handling mechanism featuring a robust data readout synchronization and event loss probability lower than 0.1% at the highest pile-up condition with a power density lower than $100\ \mathrm{mW/cm^2}$.

Summary

The front-end electronics of the CMS Outer Tracker detector presents very challenging requirements to operate in the future HL-LHC. An efficient event selection at a particle rate up to 300 pile-up requires an increase in the trigger rate and latency with respect to the existing system. Level-1 trigger requires with a fixed latency of 12.8 us the full event to be read out at an average rate of 1 MHz.

The readout of the raw full event produces a data rate of 32 Gbps that does not fit the limited output bandwidth per module of 640 Mbps. Therefore, upon the reception of a trigger, 32 sensor readout ASICs provide the zero-suppressed full event to 2 data concentrator ASICs. Zero suppression and data compression functions generate variable size event data packets while the finite datalink bandwidth and the random nature of trigger arrival times make necessary a temporary on-chip data storage. For this reason, a FIFO-based architecture has been studied and implemented.

FIFO storage elements are based on latches to reduce the overall power consumption. To accurately size FIFOs, a multichip simulation based on physics Monte Carlo samples has been performed. Although a low event loss probability is acceptable, overflow condition in a FIFO must not affect the synchronization between ASICs and with the experiment back end. Therefore, the architecture implements exception handling with error generation at different levels of the readout chain guaranteeing a robust synchronization.

This contribution will present the methodology, the analysis work and the results for sizing the data FIFOs and the implementation of FIFO overflow handling techniques using physics Monte Carlo generated events for different detector occupancy values. Simulation results provide an event loss probability lower than 0.1 % at an average rate of 1 MHz and in 300 pile-up condition with a total power density lower than 100 mW/cm2 for the readout ASICs and data concentrator ASICs.

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