A CANopen based prototype chip for the Detector Control System of the ATLAS ITk Pixel Detector

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The ATLAS experiment will get a new inner tracker (ITk) during the phase II upgrade. The innermost part will be a pixel detector. A new Detector Control System (DCS) is being developed to provide control and monitoring of the ITk pixel detector. The Monitoring Of Pixel System (MOPS) is a CANopen based Application Specific Integrated Circuit (ASIC) foreseen to independently monitor a serial power chain. The final chip is required to be radiation hard up to an ionizing dose of 500 Mrad.

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Detector Control System Overview

A new DCS is foreseen to be used in the ITk Pixel Detector. This is to ensure reliable operation of the system over the whole detector lifetime. The DCS provides three independent paths which differ in terms of availability, reliability and granularity of data they provide.

Interlock path:
- Directly acts on the power supplies
- Highest reliability (always available)

Control path:
- Provides interface to operate
- Also helps to execute calibration and commissioning
- Provides monitoring values (Temp. and Voltages)
- High reliability
- Module level granularity
- Independent power/communication lines

Requirements

- Measure temperatures and voltages for individual modules in a serial power chain
  - Expected: 15 Temperatures / 16 Voltages
- Independent monitoring while the DAQ system is not operational
- Update frequency less than 5 sec.
- CANopen application layer for data exchange with the DCS computer
- Radiation hard design up to an ionizing dose of 500 Mrad
- Working temperature range: -40 °C to +60 °C (no active cooling)
- Supported cable length of at least 60m
- Maximum package size 10 mm by 10 mm
- TSMC 65nm technology

Monitoring of Pixel System (MoPS) chip

The Monitoring of Pixel System (MoPS) is the chip designed for monitoring the voltages and temperatures of individual chips in a serial power chain. The MoPS incorporates a 1.2V low-voltage signal level CAN physical layer which requires no high supply voltages or cascading pass-device structures. The chip is powered by a single 1.2V regulator. The CAN controller uses the CAN high speed protocol with a bitrate of 125 kbit/s.

In contrast to typical applications the CANopen protocol stack is implemented in hardware rather than software. Via the object dictionary the DCS computer can access and modify the data of the MoPS chip. The control logic of the chip is triplicated to reduce the impact of single event upsets caused by the ionizing radiation. The control logic as well as the CAN controller have been successfully tested using an FPGA based setup.

Tests of the first testchip showed an excessive current draw at voltages higher than 2.8V. This current draw is due to the ESD protection structures in the pad cells becoming active at higher voltages. Therefore the amount of possible testing on the unmodified chips was limited. Two chips were modified to remove the ESD structures.

Although the removal of the ESD protection structures using a focused ion beam created unintended shorts, the results gathered from the modified chips show that the circuits work as intended. Therefore a version of the CAN physical layer and the required voltage regulators without the ESD protection structures has been submitted in August 2019. To reduce the risks associated with the high voltage present in the CAN physical layer an alternative non-standard 1.2V low voltage CAN physical layer has been developed and will be submitted with the next prototype.

Submitted Testchip & Results

The first submitted testchip contained a CAN physical layer as well as the required voltage regulators for supplying the physical layer. The CAN physical layer is composed of individual driver and receiver / monitor circuits. The developed CAN physical layer requires three separate supply voltages of 1.2V, 2.4V and 3.6V. These are derived from the single 5V input supply voltage via three voltage regulators. Similar to the CAN physical layer these voltage regulators use cascaded pass-devices to support the high input voltage of 5V. The amplifiers of all three regulators are supplied by a common 1.2V rail, which is fed from the output of the 1.2V regulator.