ATLASpix3: A high voltage CMOS sensor chip designed for ATLAS Inner Tracker


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Principle of operation of HVCMOS sensors

ATLASpix3 employs a column drain readout with trigger. It supports trigger latency up to 25us. The chip can be configured to be read out with or without trigger. In the first case, the hits are sorted chronologically. The data paths differ in each case. During triggerless readout, the hit data is shifted out from the hit buffers through the upper end of column register. In the triggered readout configuration, the hits are transferred to CAB buffers where they are filtered based on trigger signal.

Summary

ATLASpix3 is a 2 x 2 cm² monolithic sensor chip designed for ATLAS inner tracker layer 4. It employs several novel digital implementations for readout control including command decoding and clock data recovery. The specifications of the readout state machine are determined using ROME. The readout control block follows RD53A specification to ensure compatibility. ATLASpix3 is quad module compatible of which will be built within the HVCMOS collaboration. The chip is packaged and currently being tested.

ATLASpix3 simulation using ReadOut Modeling Environment (ROME) (Developed at KIT-ADL by R. Schimassek)