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# ATLASpix3 : A high voltage CMOS sensor chip designed for ATLAS Inner Tracker

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ATLASPIX3 is a 2cm x 2cm HVCMOS sensor designed to meet the specifications of layer 4, ATLAS inner tracker. ATLASPIX3 is a depleted monolithic CMOS pixel detector. The chip size allows the construction of quad modules of equal size as that of hybrid sensors. ATLASPIX3 supports triggered readout. The hit information is transmitted via 1.28 Gbit/s. The clock, trigger and configuration bits are derived from a single command input that follows RD53 protocol. This contribution will summarize the detector architecture and concentrate on the design of readout circuitry. If available, the first measurement results will be presented.

## Summary

ATLASPIX3 is a HVCMOS sensor designed to meet the specifications of layer 4, ATLAS inner tracker such as radiation tolerance of 100 MRad and 1015 neq/cm2, in-time efficiency of 99% within 25ns, power consumption of less than 300mW/cm2. Several on chip features such as sorted readout, command decoder, aurora 64b/66b encoding are implemented in ATLASpix3 compared to its small-scale predecessors ATLASpix1 and ATLASpix2. It is compatible with the hybrid pixel sensors RD53 ASIC in terms of electronic interface and geometry.
ATLASPIX3 is a depleted monolithic CMOS pixel detector implemented in 180nm high voltage CMOS technology. Instead of standard substrate, we use a high ohmic substrate of resistivity 200-Ohm cm. The chip size is 2cm x 2.1cm, which allows the construction of quad modules of equal size as that of hybrid sensors. 90% of the chip area is active with 10% periphery at the bottom. The pixel pitch is 50µm x 150µm. ATLASPIX3 supports triggered readout with programmable latency up to 25µs. The hit information (pixel address, 10 bit time stamp and 7 bit amplitude information) is transmitted via 1.28Gbit/s digital link. The interface is based on a single command input that is used for providing clock, trigger and configuration commands. The command protocol is the same as that of RD53. The chip has been submitted and we expect the first results in August.
This contribution will summarize the detector architecture and concentrate on the design of digital blocks: hit buffers, trigger buffers, readout control unit, command decoder and clock generator. If available, first measurement results will be presented.

**Primary authors:** PRATHAPAN, Mridula (KIT - Karlsruhe Institute of Technology (DE)); PERIC, Ivan (KIT - Karlsruhe Institute of Technology (DE)); ZHANG, Hui (Karlsruhe Institute of Technology (KIT)); WEBER, Alena Larissa (Ruprecht Karls Universitaet Heidelberg (DE)); WONG, Winnie (Universite de Geneve (CH))

**Presenter:** PRATHAPAN, Mridula (KIT - Karlsruhe Institute of Technology (DE))

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