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The eTx line driver and the eRx line receiver: two building blocks for data and clock transmission using the CLPS standard

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This paper presents the design and test results for the line driver (eTx) and the line receiver (eRx) in the lpGBT, fabricated in 65 nm CMOS technology. The two circuits implement the physical layer of the bi-directional eLink interface of the lpGBT. The eTx is a single-ended-to-differential driver with programmable pre-emphasis and driving current. The eRx is a differential-to-single-ended receiver with programmable line equalization. Both circuits comply with the CERN Low Power Signaling (CLPS) standard and have been qualified for data transmission up to 1.28 Gbps.

Summary

The eTx and eRx circuits are part of the lpGBT chip that is used to implement multipurpose high-speed bidirectional optical links for high-energy physics experiments. The eTx and eRx implement the physical layer of the eLink interface in the lpGBT for data and clock transmission between the lpGBT and the front-ends. In this paper, we will discuss the designs, usages and test results of the eTx and the eRx, which have been fabricated in a 65nm CMOS technology and tested as part of the lpGBT.

The eRx block occupies an area of 210 □m □ 80 □m including the eRx core, ESD circuits and on-chip decoupling capacitors. The eRx core is designed to accommodate a rail-to-rail input common voltage range (0 to VDD = 1.2V) and a differential amplitude between 140 mV and 800 mV. On-chip termination resistors and a default input common voltage (Vdd/2) can be enabled or disabled within the eRx to adapt to different system topologies including AC coupling and multiple drop configurations. A passive line equalization at the input of the eRx core provides four preset peaking transfer functions (including "flat-band"). Parallel PMOS and NMOS input differential stages are used to achieve rail-to-rail operation and a self-bias structure is employed in the eRx core to simplify the bias circuits. The whole eRx power consumption is 850 □W (typical) when working at 1.28 Gbps.

The eTx block is designed to operate up to 1.28 Gbps for data transmission (extending beyond the lpGBT downlink eLink data rates) and up to 1.28 GHz for clock transmission. It adopts the Source-Series-Terminated (SST) structure for low power operation and outputs differential signals with 600 mV (VDD/2) common voltage and programmable differential amplitude between 200 mV and 800 mV (typically) when using an external 100 Ohm termination. The eTx also features programmable pre-emphasis. Both the peaking strength and the peaking time duration are programmable.

The lpGBT chip was taped out in July 2018 and testing has been conducted from April 2019. Both the eRx and eTx blocks were verified as part of the lpGBT and perform according to specifications. Besides discussing in detail the architecture of both circuits, the experimental results including those of the irradiation tests, that will take place during the Spring 2019, will also be presented during the conference.

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