Contribution ID: **17** Type: **Poster**

COLDATA Architecture, Design and Verification

Tuesday 3 September 2019 17:20 (20 minutes)

COLDATA is the third of three chips designed for operation within the Liquid Argon cryostat of the Deep Underground Neutrino Experiment (DUNE). It is the point-of-contact between the warm, external DUNE DAQ system and the cryogenically-cooled Front-end Boards. All information from warm-to-cold and from cold-to-warm passes through COLDATA. As such, it implements data concentration and frame formation, slow control communication and relay, fast control communication, clock distribution and readout. With so much communication, extensive verification was essential. The following will present the complete COLDATA architecture as well as its unique Verification Plan accomplished following the Universal Verification Methodology.

Summary

The Deep Underground Neutrino Experiment (DUNE) intends to place its front inside a multi-kiloton liquid argon tracking calorimeter located more than a kilometer underground at the Sanford Underground Research Laboratory in Lead, South Dakota. Such an ambitious endeavor required considerable design effort in every area from lifetime and reliability to data transmission and cable mass. Signals from the Time-Projection Chamber are amplified and shaped by the LARASIC, a front end consisting of16 channels per chip and then digitized by coldADC, a 12 stage pipelined Analog to Digital Converter.
The purpose of COLDATA isS act as the gatekeeper and data concentrator for the front-end chips. As it is immersed in LiAr, the chip is operating at a cryogenic temperature of ˜87k. It communicates with the external DAQ system through a minimal set of copper wires, including a differential pair for a 64MHz clock (shared between two COLDATA chips), a differential pair for a fast command (shared between two COLDATA chips), three differential pairs for I2C slow control (SCL, SDAin and SDAout), and two differential pairs for data readout.
The principle responsibilities of the COLDATA are as follows:
1. To generate and distribute 2MHz Sample clocks and 64MHz clocks to each of the coldADC chips.
2. To relay I2C commands and responses to and from the coldADC chips under its jurisdiction and to a neighboring COLDATA chip. It must also respond to I2C commands if those commands are directed at the COLDATA chip itself.
3. To respond to a limited set of fast commands (e.g. reset, calibrate, etc) in a time-sensitive manner.
4. To act as a cryogenic repository for all data to be programmed to the LARASIC chips and to download that data to the LARASIC chips when required by the DAQ system.
5. To capture all data from the coldADC chips and frame that data by sample period in one of several user selectable frame types.
6. Finally, to deliver the captured data to the DAQ system through the two differential readout lines at a rate of 1.28Gbps. The readout frequency is generated from MEMS oscillators located on the front-end boards and a PLL integrated on the COLDATA chip. The data readout signals are driven across 25+ meters of copper cable by CML drivers also integrated on the COLDATA chip.
The development of COLDATA comes after extensive transistor cryogenic lifetime analysis of available technologies and the design of complete libraries based on design rules extracted from the lifetime analysis. The verification of the COLDATA chip was quite extensive, simulating all manner of changing, real-life scenarios. This was made possible through the Universal Verification Methodology and System Verilog Assertions.

In particular, since the COLDATA must communicate with coldADCs and other COLDATA chips, the novel approach was taken to treat the entire front-end board as the device under test and simulate genuine communication between all of these chips rather than verifying a single COLDATA chip as would by more typically done.

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Session Classification: Posters

Track Classification: ASIC