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Coming challenges for Photon Science detectors: an ASIC designer perspective

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Coming developments in X-ray photon sources will increase signal rate and intensity. Similar performance improvements are needed in a new multi-mega pixel imager. Its readout ASIC is to be based on charge-integration, be compatible with different sensor types, include adaptive-gain (to achieve single-photon resolution and high dynamic range), radiation-hard solutions and circuits for rapid characterization. On-chip digital conversion is desirable; readout should happen indefinitely at over 100kfps rate.

It is our intention to present challenges and ideas, to get advantage of the expertise of the HEP community to look for solutions that could be applied to the Photon Science field.

Summary

Coming developments in X-ray photon sources will provide improvements in terms of average signal rate and intensity. Upgrades of Storage Rings to Diffraction Limited operation is expected to increase brilliance by two orders of magnitude. At the same time, upgrade of superconducting-linear-accelerator-based Free Electron Lasers to Continuous Wave operation might slightly reduce burst-bunch-rate, but will speed-up average-bunch-rate up to $10^5 \sim 10^6$ per second.

Similar performance improvements are needed in detectors to cope with upgraded sources. It is our opinion that these challenges are best answered with the development of a new multi-mega pixel imaging detector (in the form of a Hybrid Pixelated Array), with a frame rate of over 100k frame/sec and a dynamic range from single photon sensitivity to $10^4 \sim 10^5$ photon/pixel/image.

Its readout ASIC is to be based on a charge-integrating scheme, to cope with the expected high photon flux. Both electron- and hole-collection capability is needed in the readout circuit, to take advantage of the sensor (conventional Si, low gain avalanche, high-Z) most appropriate for a given photon energy range (respectively $\sim 10\text{keV} / \sim 1\text{keV} / 60 \sim 100\text{keV}$).

An adaptive gain scheme (operating in real time, independently for every pixel) is needed to achieve single-photon resolution in low flux condition (down to a few keV), while avoiding saturation in highly illuminated pixels, and remaining below Poisson noise.

Correlated Double (and when needed, Multiple) Sampling, low-noise circuitry and Programmable Gain Amplification selection should be included in the pixel architecture; radiation hard solutions (by enclosed gate layout or equivalent) need to be used to harden key circuits against radiation damage, to mitigate performance degradation.

On-chip digital conversion is highly desirable: signal processing and readout should be able to happen indefinitely at a rate exceeding 100k frame/s (rather than being limited by an internal memory as happens today in fast detectors for FEL), with minimal or no dead time (Continuous Read-Write operation). Embedded circuits for rapid characterization and calibration of devices in realistic environments also need to be included, ideally in different points of the readout chain.

A pixel pitch between 50 and 100 μm seems a reasonable compromise between spatial resolution and signal-processing needs, as four-side-buttability (prerequisite for modularity and ease-of-replacement) calls for minimization of peripheral insensitive areas.

Power consumption (and heat dissipation), readout line parallelization and efficient ways to deal with the

sensor output (which can easily exceed 100 Gbit per ASIC) need to be considered as well.
It is our intention to present these challenges and ideas, with the aim of getting advantage of the expertise of the HEP community to look for solutions that could also be applied to the Photon Science field.

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