ALTIROC2, a readout ASIC for the High Granularity Timing Detector in ATLAS

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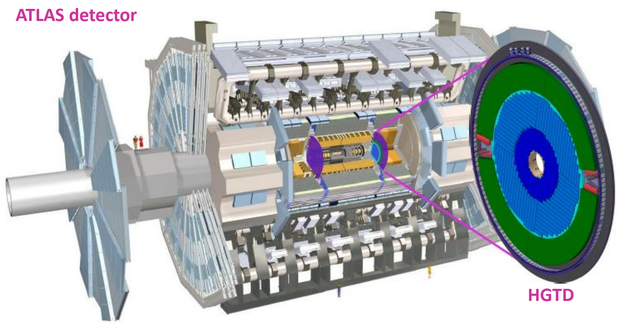
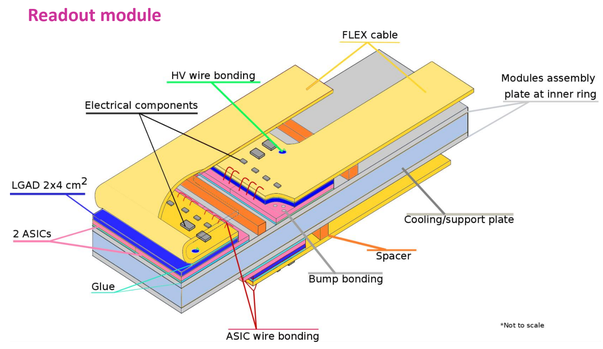
HGTD

The increase of pileup will be one of the main challenges in the High-Luminosity LHC. A way to mitigate the effects of the pileup is the use high precision timing information to distinguish between collisions very close in space but well separated in time. A High-Granularity Timing Detector (HGTD) has been proposed for the ATLAS Phase II Upgrade. It will provide a precise timing information (30ps per track) and a measure of the luminosity per bunch crossing.

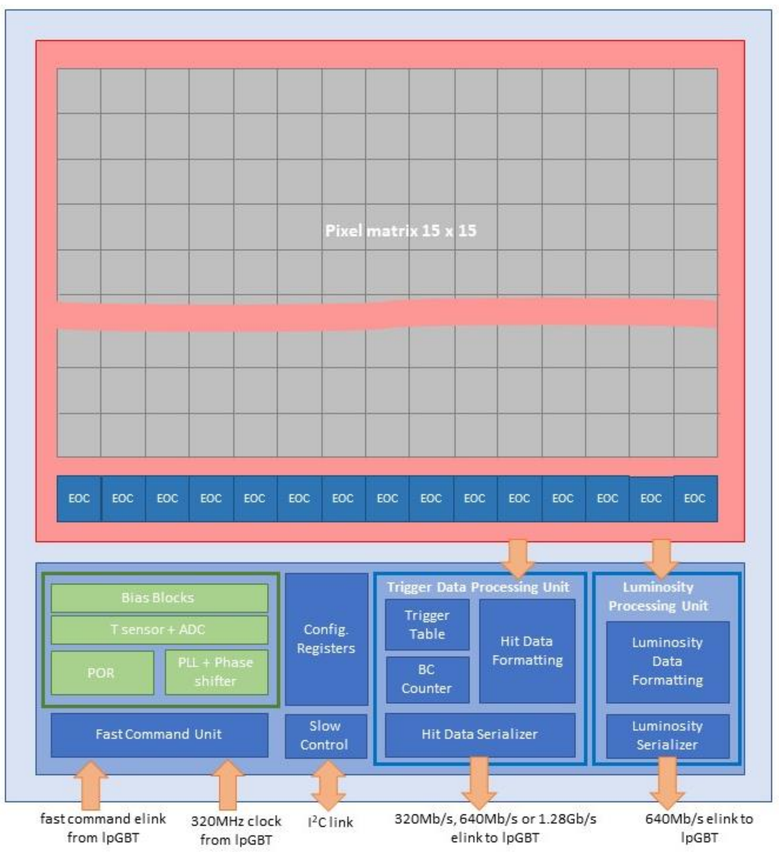


Two HGTD detectors will be placed at the end-cap regions. Each HGTD is a disk composed of two layers of very thin (50µm) Low Gain Avalanche Diodes (LGAD) with a pad size of 1.3x1.3mm^2. The disks are equipped with staves of different length. Each stave is composed of modules of 2 x 4 cm^2 which contain:

- 1 sensor array of 450 LGADs with a size of 2x4cm^2.
- 2 readout ASICs.
- Sensors and ASIC connected through bump bonds.



ALTIROC2 architecture overview



Main features

- ALTIROC2 is designed to readout 225 LGAD sensors.
- Sensor readout electronics integrated in an area of 1.3x1.3mm^2.
- ALTIROC2 performs 2 measures:
  - **Timing:** time of arrival (resolution of 30ps) and time over threshold of each detected hit per pixel.
  - **Luminosity:** number of hits in all the channels per bunch crossing.
- Small contribution to the timing resolution to match the excellent performances of the LGADs. Contributions due to:
  - **Time-walk:** addressed by correcting the time of arrival with a measure of the time over threshold.
  - **Jitter:** addressed by optimizing the analog front-end electronics.
- The time information is readout on the reception of a trigger. Two working scenarios:
  - **L0 scenario:** maximum rate of 1MHz and latency of 10µs.
  - **L0/L1 scenario:** maximum rate of 800kHz and latency of 35µs.
- Data transmitted through e-links to an lpGBT ASIC

Pad size	1.3 x 1.3 mm^2
Detector capacitance	3.4 pF
TID and neutron fluence	Inner region: 4.1 MGy, 3.7 x 10^{15} n$_{eq}$/cm^2 Outer region: 1.6 MGy, 3.0 x 10^{15} n$_{eq}$/cm^2
Number of channels/ASIC	225
Collected charge (1 MIP) at gain = 20	9.2 fC
Dynamic range	1-20 MIPs
(preamplifier + discr.) jitter at gain = 20	< 20 ps
Time walk contribution	< 10 ps
TDC binning	20 ps (TOA, TZ TOT), 40 ps (VA TOT)
TDC range	2.5 ns (TOA), 5 ns (TZ TOT), 10 ns (VA TOT)
Number of bits/hit	7 for TOA and 9 for TOT
Luminosity counters per ASIC	7 bits (sum) + 5 bits (outside window)
Total power per area (ASIC)	< 300 mW/cm^2 (< 1.2 W)
E-link driver bandwidth	320 Mb/s, 640 Mb/s or 1.28 Gb/s
Latency for L0/L1 triggering	10/35 µs

Fast command unit

- Fast commands: GRST, L0A, L1A, …
- Serial data transmission at 320Mb/s (one command every 25ns).
- lpGBT e-link.
- Generates an internal clock of 40MHz from a source clock of 320MHz passed by lpGBT.

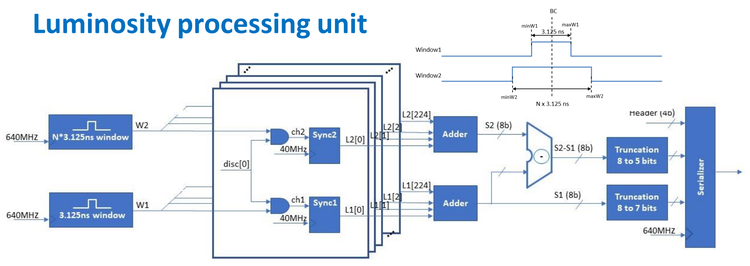
Slow control

- I^{2}C link to access 8-bits configuration registers: pixels, windows, clock phase, …
- Data rate: compatible with 1MHz standard speed.
- I^{2}C and configuration registers. connected through a Wishbone bus.
- 1024 configuration registers.

Trigger processing unit

- Fast commands are processed by the trigger data processing unit. This is responsible for:
  - Reading the timing information from the pixel matrix.
  - Pack data into frames.
  - Serialization.
- Main blocks:
  - 12-bits bunch crossing counter.
  - Trigger table to store temporally received trigger commands for later processing.
  - Data formatting unit to pack data into frames.
  - Serializer.
- When an L0A/L1A command is received :
  - An internal trigger signal and a trigger identifier are generated and immediately passed to the pixel matrix.
  - Trigger identifier and current bunch crossing stored into a trigger table.
- Steps performed for data readout:
  - Fetch a new entry from the trigger table.
  - Request to the EOCs to retrieve data from the pixels related to the trigger event fetched from the table. Retrieved data is stored temporally in the EOC.
  - Data are transferred from the EOC to the trigger data processing unit, where they are packed into frames, serialised and transmitted.

Luminosity processing unit



- **Luminosity:** number of hits within a time window per bunch crossing.
- 2 time window centred on the bunch crossing:
  - *W1*: width of 3.125ns.
  - *W2*: width multiple integer of 3.125ns.
- Two luminosities *S1* and *S2* corresponding to *W1* and *W2* respectively are measured.
- Windowing performed in pixel.
- Luminosity processing unit:
  - Calculates *S1*, *S2* and then performs *S2-S1*.
  - Truncated due to bandwidth limitations. *S1* to 7bits and *S2-S1* to 5bits.
  - Serialization and transmission of *S1* and *S2-S1* per bunch crossing.
  - Frames length: 16bits.

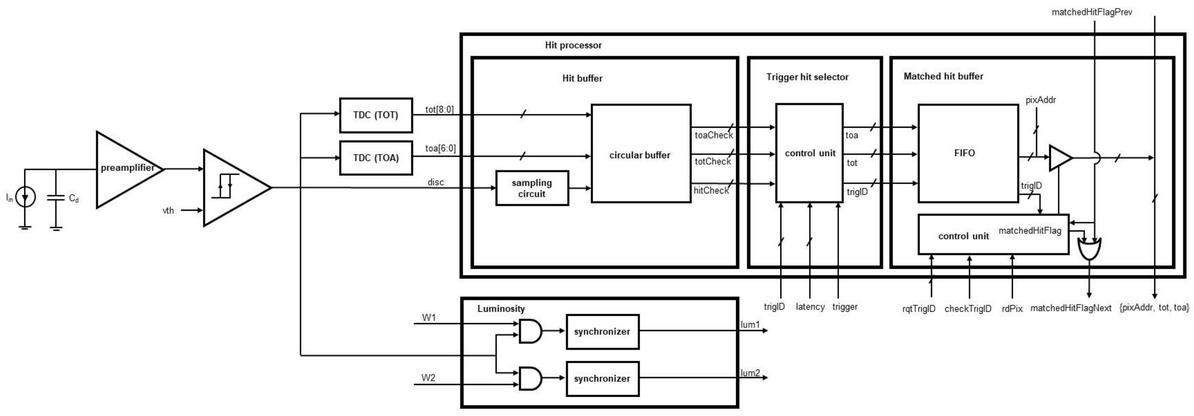
Data transmission

- The amount of data to transmit depends on the radial position of the ASIC in the detector.
  - Timing:
    - average hit rate for R < 150mm: < 30hits ➡ 1.28Gb/s
    - R > 150mm ➡ 320Mb/s
  - Luminosity:
    - only data from ASICs at 320mm < R < 640mm to limit bandwidth requirements
    - average hit rate < 40hits + 16b/BX ➡ 640Mb/s

Clock distribution

- Digital circuits work at 40MHz except serializers, window generators, and the EOCs.
- PLL to generate different clocks:
  - 80MHz: for the communication between the EOC and trigger data processing unit
  - 320MHz: serializer
  - 640MHz: serializers, window generators
- Phase shifter to adjust the phases of the internal clocks
  - Shift step: 100ps
  - Jitter < 5ps

In-pixel electronics



Analog front-end stage

- Voltage preamplifier + fast discriminator.
- Time walk correction made with a TOT architecture. Smaller than 10ps over 10MIPs dynamic range after correction.
- Two TDCs (Time to Digital Converters) to provide TOT + TOA measurement:
  - TOA: range of 2.5ns and a bin of 20ps (7bits).
  - TOT: range of 20ns and a bin of 40ps (9bits).
- Preamplifier optimized to minimize the electronics jitter below 25ps for an input charge of 10fC and detector capacitance of 4pF.

Digital electronics

- **Hit buffer** stores the timing information of each bunch crossing until a trigger arrives:
  - Circular buffer: 1400 positions to store hit/no hit, TOT and TOA
  - TOT and TOA only stored when a hit is detected to save power
  - SRAM: 1400 x 19bits
  - Control unit to handle the read and write pointers of the circular buffer
- **Trigger hit selector** checks if data related to a trigger event is stored in the hit buffer.
  - Each received trigger has associated a trigger identifier.
  - If data related to the received trigger are found in the hit buffer, these are stored with the trigger identifier in the matched hit buffer
- **Matched hit buffer** temporally stores the timing information of those hits associated to a trigger event:
  - FIFO:32 positions to store TOT, TOA, and trigger identifier
  - Control unit: looks for data related to a trigger event in the FIFO when requested by the EOC
  - Matched flag handled through a priority OR chain for readout. Pixel at the top of the column has the higher priority.
  - Synchronous readout at 40MHz
- **Luminosity** checks if every detected hit is inside two programmable windows *W1* and *W2*.
- **Configuration registers**