A Monitoring 12-bits Fully Differential Second Order Incremental Delta Sigma Converter ADC for TimePix4

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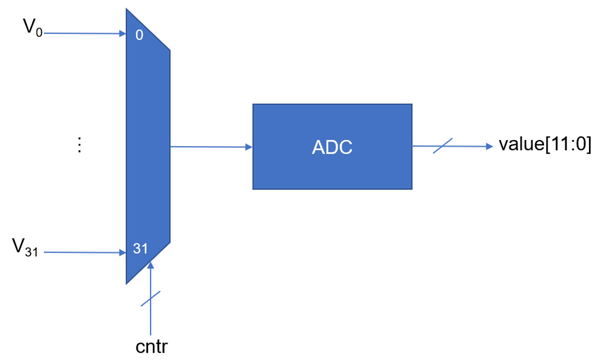
Introduction

SAR converters are usually the natural choice to implement monitoring ADCs. Additional circuits for calibration are needed to compensate process variations which become more important for high resolutions and in deep-submicron technologies. This poster presents a 12-bits second-order incremental sigma delta converter for TimePix4 fabricated in TSCM 65nm. It does not need calibration and is robust to process variations because most of the signal processing is performed in the digital domain. It provides a maximum conversion rate of 1kHz/s, enough for monitoring the internal signals of the chip, consuming only 8µW. Simulations show a SNR of 84.9dB operating in free-running mode.

Requirements

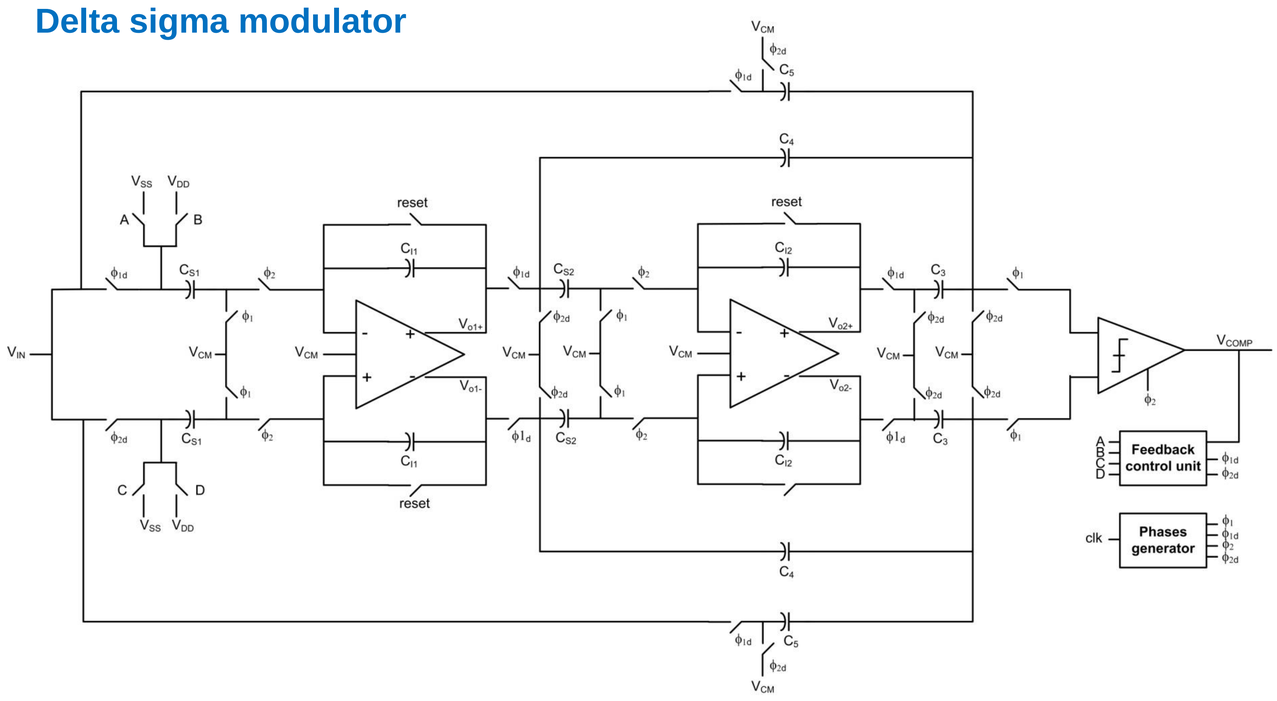


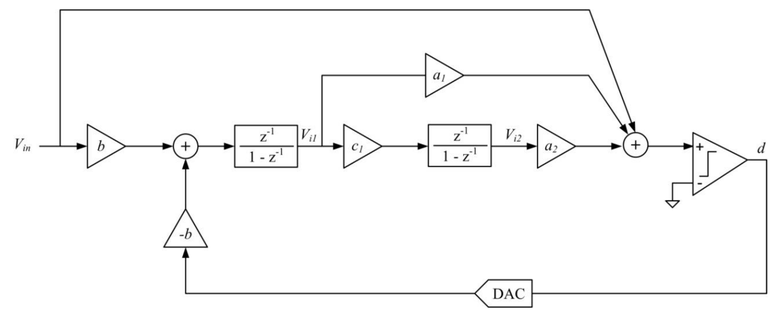
- Monitoring of internal bias voltages
- 32 channels multiplexed
- Resolution: 12 bits
- Max. speed: 1000 samples/s
- Power supply: 1.2V

Incremental Delta Sigma Converter

- Delta sigma converters offer high resolution and moderate speeds.
- Most of the digital processing is performed in the digital domain:
  - Robust to analog parameter variations
  - Technologically scalable
- Incremental Delta Sigma converters can be considered delta sigma converters operating in transient mode which can be reset periodically.
- Main features:
  - Sample to sample conversion
  - Provide high resolution
  - Low offset and gain errors
  - Resetable (it can be multiplexed between multiple channels)

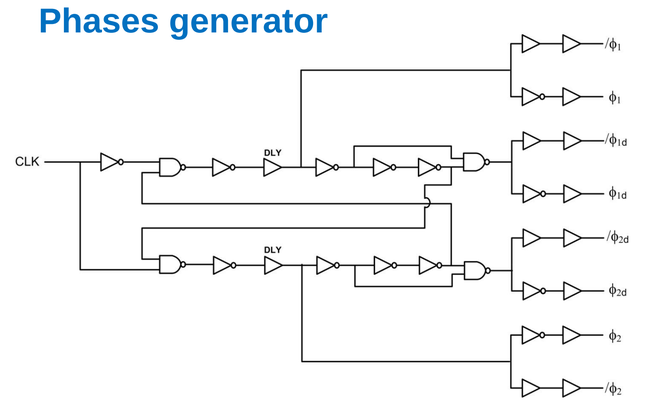
Delta sigma modulator



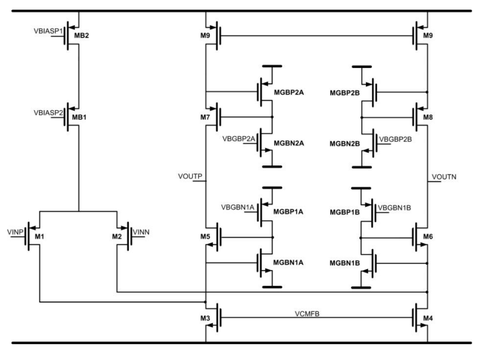


- 2nd order Cascaded Integrators Feed Forward (CIFF) architecture:
  - Tradeoff between area, conversion speed and power consumption
  - Less sensitive to non-linearity of the integrators
  - Less voltage swing at the output of the integrators
  - Only one feedback DAC is needed.
  - Signal Transfer Function is 1
- Coefficients and main characteristics of the opamp obtained by simulation with SIMSIDES

Phases generator

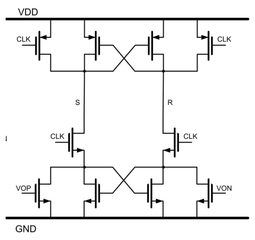


Operational amplifier

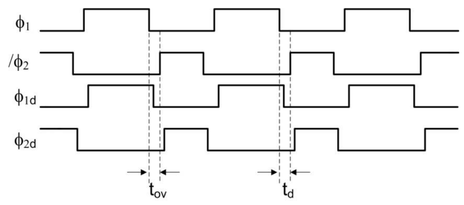


- Folded cascode + gain boosting Switched capacitor CMFB circuit
- A_{OL} = 85dB
- GBW = 5.7MHz (@0.5pF)
- PM = 87º (@0.5pF)

Comparator

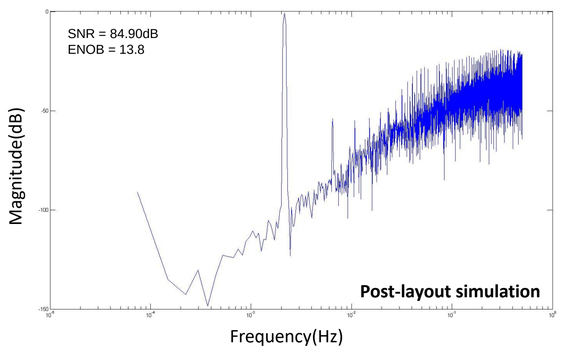


- Dynamic latch:
  - zero DC current in reset mode
  - S and R both precharged to VDD
  - full logic level after regeneration
  - slow
- SR latch connected to the S and R outputs



Simulations and Layout

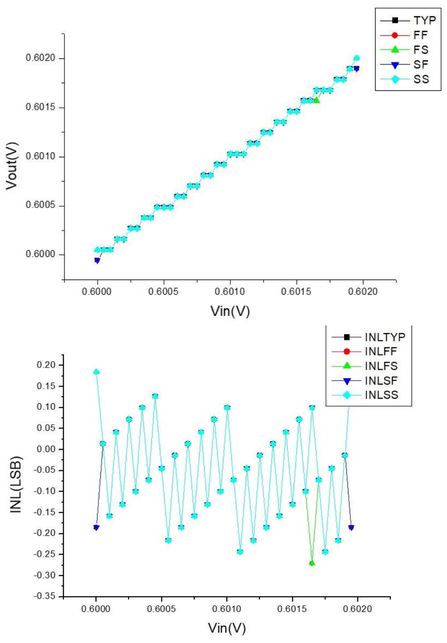
Free running mode



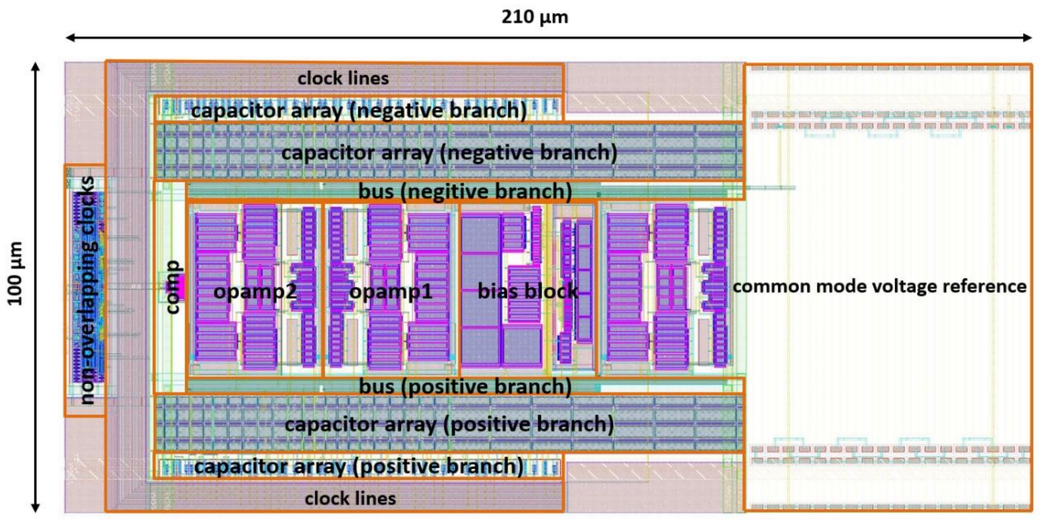
Corner	SNR (dB)	ENOB
Typical	84.90	13.9
SS	89.19	14.52
FF	80.37	13.06

- Sinusoidal input signal:
  - Amp:0.55 V
  - Freq. 543 Hz
- OSR = 210
- FFT: 64 * 210
- Simulation time: 2 days

Normal mode



- Not possible to simulate the whole dynamic range (long simulation time)
- Only small regions analzsed



Main features	
Bias voltage	1.2V
Full scale voltage	1.1V
Resolution	12bits
Max. conversion rate	1190samples/s
Power consumption	3.5µW (Delta sigma modulator) 4.5µW (VCMRF) **Total:** 8µW
OSR	210
Max. oversampling frequency	250kHz