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A Monolithic Active Pixel Sensor for CEPC vertex detector

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The proposed CEPC presents new challenges for the pixel detector in terms of cell size and functionality. A high data rate digital design and readout architecture of a MAPS prototype for the CEPC vertex detector is presented. The column drain based readout architecture, benefiting from the ALPIDE and FE-I3 approach, has been implemented to achieve high spatial resolution, fast readout, and low power consumption. The simulation results indicate the readout logic works properly with the high input data rate of 120MHz; both analogue front end and in-pixel readout logic meet the 25ns bunch spacing.

Summary

The Circular Electron-Positron Collider (CEPC) is proposed for high-precision measurements of the Higgs boson. It will include a vertex detector designed to provide an excellent impact parameter resolution. Monolithic Active Pixel Sensors (MAPS) are being investigated for the CEPC vertex detector due to its high granularity, high speed, low material budget, low power consumption and radiation tolerance. According to the preliminary estimation, radiation hardness requirements will be of ˜1MRad/year and 2×1012 1MeVneq/cm2/year for Total Ionizing Dose (TID) and Non-Ionizing Energy Loss (NIEL) respectively. The previous MOST1 project resulted in the first prototype of 25×25μm2 pixels was produced with a 0.18um CIS process from TowerJazz. However, the analogue peaking time (1μs) and integration readout time (100μs) of the MOST1 did not meet the requirement. In order to overcome those limitations, the MOST2 was launched in 2018. The first prototype with a pixel matrix of 192×64 has been submitted to fabrication in June 2019 and it is presented in this paper.

This new prototype includes several enhancements. The analogue front end has been optimized for fast rising time (<25ns) and two new fast in-pixel readout logics have been designed: an FE-I3 like scheme and ALPIDE scheme. In the first readout logic, the electronics are very similar to those of the FEI3 but due to area limitations, the address ROM has been replaced by a simplified address generator array and the timestamp is not stored in-pixel but at the End Of Column (EOC). In the ALPIDE pixel, the electronics are the same but the hit storage registers have been replaced by an edge-triggered flip-flop in order to reduce the global control signal for less area occupancy and the priority Address Encoder and Reset Decoder (AERD) block has been modified to boost its speed to 40MHz. The pixel matrix is subdivided into two matrices of 96×64 pixels, each one with a type of pixel flavor so that their performances and challenges can be addressed in direct comparison. Both schemes employ the same double column drain architecture. The pixel readout is arbitrated by a token propagation, with the topmost pixel having the highest readout priority. At the EOC, the circuitry has a counter running at 40MHz to generate the timestamp with 25ns steps; the data will match the timestamp and be stored temporally for each double column in the first level FIFO, then the data will be suppressed to eliminate mismatched timestamps with the trigger mode and transmitter to a serializer buffered by the second level FIFO. Triggerless mode is also supported to preserve all the readout data before buffering to the output. In order to implement a high-speed serialization transmission, the clocks are managed by a Phase Lock Loop (PLL) which offers up to 4Gbps data rate capability.

In this work, the prototype mentioned above will be described and the preliminary simulation results will be presented.

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