The ETROC Project: Precision Timing ASIC Development for LGAD-based CMS Endcap Timing Layer (ETL) Upgrade

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ABSTRACT

The ETROC (Endcap Timing Readout Chip) is being developed for the LGAD-based CMS Endcap Timing Layer (ETL) at LH-LHC. The ETL on each side of the interaction region will be instrumented with a two-board system of MP-sensitive LGAD silicon devices to be read out by ETROCs for precision timing measurement with down to 30 ps timing resolution. The ETROC is designed to handle an 18 x 16 pixel matrix, with each pixel being 1.3 mm x 1.3 mm to match the LGAD sensor pixel size. Approximately 15% of the sensors near the highest eta region will experience hadron fluence above 1e15 mev/cm^2 towards end of operation of HL-LHC, resulting in small signal amplitude with LGAD gain reduced to around 10. For this reason, the front-end design for preamplifier and discriminator has been specifically optimized for the reduced LGAD signals, with enough flexibility to meet the ETL specific needs for time resolution, power budget, and radiation tolerance of the ASIC.

The ETROC chip is implemented in TSMC 65nm. At the pixel level, each channel consists of a preamplifier, a discriminator, a TDC used for TOA (time of arrival) and TOT (time over threshold) measurements, and a memory for data storage and readout. The TOT is used for time-wall correction of the TOA measurement. The detailed hit information (TOA and TOT) from within each cell will be read out by a local circular buffer after each level-1 Accept (about 1 MHz). In addition, a charge injection circuit is implemented to allow for testing and calibration. For more detailed monitoring of the signal pulse as rise time increases, waveform sampling circuits will be included in selected pixel cells. Additional peripheral circuits include a PLL, a phase shifter, a 12C slave, a fast control block, a serializer, and a data driver. The main design challenge is how to extract precision timing information from the small LGAD signals in the presence of high irradiation fluence, while keeping the power consumption low. The ETL design guidelines for the time resolution of 50 ps per hit is required in order to achieve a 35 ps arrival time measurement for a MP particle, which has its track registered in two ETL disk layers. The LGAD contribution is known to be about 30 ps, this means that the jitter from the ETROC has to be kept below 40 ps.

ETROC DEVELOPMENT STAGES

ETROC: single channel with preamp + discriminator
ETROC1: low power TDC and 4x4 clock tree ETROC2: 16x16 full size chip

ETROC1 single pixel layout

ETROC0: PREAMPLIFIER and DISCRIMINATOR

The goal of the ETROC design is to translate the performance of the preamplifier and discriminator. The ETROC is a single channel design which consists of a preamplifier with adjustable gain limited by a discriminator with a user programmable threshold controlled in a digital manner.

The preamplifier has two-stage design. A cascode amplifier with feedback resistors acts as the first stage, and output follower as the second stage. The size of each transistor in the second stage has been optimized by using LGAD simulation as the input signal. The design considers both feedback and noise. The transistor size is selected for the best performance. The feedback resistors are programmed to allow adjustment of the full scale, while the size of current is also programmable to allow different tradeoffs between power consumption and performance by setting the value of the current.

The threshold for the discriminator is optimized for the best noise for low signal input while keeping power consumption low.

LGAD + ETROC expected system performance

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WAVEFORM SAMPLING

For the robust long term operation of the ETL, it will be important to continuously monitor the performance of this readout system. Several waveform sampling techniques are available and can be used in the ETROC to monitor the performance of the LGAD sensors. One approach is to use the preamplifier to measure the waveform for each channel, allowing for the separation of the signal from the noise. The waveform samples can be taken at fixed intervals, or triggered by the arrival of a signal.

This can be implemented using an existing 16-bit ADC design block in silicon. The Xilinx FPGA E Block for waveform sampling in the ETROC can be a 16-bit 160 MSample/s waveform sampler which interfaces 4 channels of the 1200 MHz 12-bit high-speed ADC. A single channel 1200 MHz 12-bit ADC prototype chip, implemented in silicon CMOS process for the FPGA has been designed and tested in Aug 2018. The design uses a 14-bit 200 MHz rate waveform sampling circuit to keep it as a low power design.

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Preparation for beam test at Fermilab in Dec 2019

The ETROC Block Diagram

Prepertation for beam test at Fermilab in Dec 2019

Simulation and Chip Testing

Prepertation for beam test at Fermilab in Dec 2019