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The ETROC Project: ASIC development for CMS Endcap Timing Layer (ETL) upgrade

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The Endcap Timing Readout Chip (ETROC), being developed for the CMS Endcap Timing Layer (ETL) for HL-LHC, is presented. Each endcap will be instrumented with a two-disk system of MIP-sensitive LGAD silicon devices to be read out by ETROCs for precision timing measurements. The ETROC is designed to handle a 16×16 pixel cell matrix, each pixel cell being 1.3x1.3 mmˆ2 to match the LGAD sensor pixel size. The design of ETROC, with its unique challenges and how they are addressed, as well as prototype testing results, are presented.

Summary

The ETROC is implemented in TSMC 65nm. At the pixel level, each channel consists of a preamplifier, a discriminator, a TDC used for TOA (time of arrival) and TOT (time over threshold)
measurements, and a memory for data storage and readout. The TOT is used for time-walk correction of the TOA measurement. The detailed hit information (TOA and TOT) from within each cell will be read out from a local circular buffer after each Level- 1 Accept (about 1 MHz). In addition, a charge injection circuit is implemented to allow for testing and calibration. For more detailed monitoring of the signal pulses as radiation dose increases, waveform sampling circuits
will be included in selected pixel cells. Additional peripheral circuits include a PLL, a phase shifter, an I2C slave, a fast control block, a serializer, and a data driver.

The ETL design goal for the time resolution is 50 ps per hit, in order to achieve a 35 ps arrival time measurement for a MIP track with an ETL hit in each of the two-disk layers. This means that the jitter from the ETROC preamplifier/discriminator has to be kept below 40 ps. The main design challenge is how to extract precision timing information from small LGAD signal size due to high irradiation fluence while at the same time keep the power consumption low. Approximately 15% of the sensors near the highest eta region will have more than 1e15 neq/cmˆ2 towards end of operation of HL-LHC, resulting in small signal size with LGAD gain reduced to around 10. For this reason, the front-end design for preamplifier and discriminator has been specifically optimized for the small LGAD signals, with enough flexibilities to meet the ETL specific needs for time resolution, power budget and radiation profile. In addition, the TDC stage design has been optimized for low power operation in such a way that one simple delay line with uncontrolled delay cells is used to measure both TOA and TOT at the same time. This is made possible by using an in-situ delay cell self-calibration technique, that is, to use two consecutive rising clock edges to record two time stamps for each hit. The time difference between the two time stamps is the known clock period, and this fact can be used for delay cell calibration for every hit. Effective clock distribution is a challenge and care must be taken in minimizing clock skew and jitter. For ETROC we have adopted the most common and conservative clock distribution
scheme, known as H-tree.

The most critical component, the front-end preamplifier and discriminator, has been implemented in single channel ETROC0 and submitted in Dec. 2018. The testing of the ETROC0 has been on-going since April 2019. The TDC design has been fully implemented and is being integrated in a 16-
channel ETROC1 chip, with a 4x4 clock tree distribution. The ETROC1 chip is scheduled to be submitted in summer 2019. The waveform sampling block is being implemented as well and scheduled for submission over summer 2019.

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