Introduction

The discovery of Neutrinoless double beta decay ($0
νββ$) would prove the Majorana nature of neutrinos, and prove whether the the lepton number conservation is violated.

Among the current and planned experiments of $0
νββ$, the high-pressure gaseous Time Projection Chamber (TPC) stand out for excellent energy resolution, very low radio background active level and good scalability.

Moreover, high position resolution can be maintained with an appropriate charge readout scheme for gaseous TPC to further suppress the background through ionization imaging.

A pixelated charge readout plane without gas-electron avalanche is desirable. Based on a 0.35um CMOS process, a low noise sensor, Topmetal-S, is being developed which, even without gas gain, the 1% FWHM energy resolution requirement could be met.

Since $0
νββ$ tracks are extended to tens of cm in high-pressure gas, and taking advantage of the charge focusing electric field, the first prototype of Topmetal-S is designed to have nm-sized charge collection electrode, followed by a charge sensitive amplifier and an ADC in the first prototype.

To realize a ton-scale high-pressure gaseous TPC, approximately one hundred thousand Topmetal-S sensors need to be laid on a meter-sized plane. The greatest challenge is a reliable high-density sensor readout and sensor control.

• To pass through.

• Fault node detection is implemented by sending test packets by the computer.

• After fault detection, through sending configuration command packets the computer will form a set of orthogonal region called faulty blocks to contain detected faults.

• The FT-XY routing follows the regular XY routing until the packet reaches a boundary node of a faulty block.

• At that point, the packet is routed around the block clockwise to pass through.

The Network Design

The topology of readout network

• The noise of the CSA is about 30e-.

• The sample frequency of the ADC is 25.5 MHz. After a four-order 64-times oversampling Cascaded Integrator-Comb decimation digital filter, the effective sampling rate of the ADC is 400 Ks/s with a 14 effective number of bits at a 200 KHz input signal.

The topology of readout network:

• Stores the configuration of SPI.

• Generates the test data packet based on the configuration of SPI.

• The south interface is used to receive the data generated by the sensor itself, the other direction ports are used for the data forwarding.

• Used to receive the data generated by the sensor.

• By the computer.

• Generates data to simulate the data generated by the detector of the sensor, and analyzes the received data packet.

• FPGA prototype verification structure for a 10×10 network

• The PC generates data to simulate the data generated by the detector of the sensor, and analyzes the received data packet.

• Test packet fifo will receive the data from Ethernet, and then send the data to a node in the network through the local port of a router.

• The receiver will receive the data output at the network boundary node and send it to the Ethernet module.

FPGA prototype verification structure for a 10×10 network

• Serial throughput rate per boundary node is 36.64Mbit/s

• The throughput of a 10×10 network has reached 368.4Mbit/s.

• The maximum delay of a 10×10 network is 7.6us

The FPGA verification and the Router prototype

The router design

• The router prototype chip consists of a router module and a debug module for chip test.

• Based on the destination address information carried in the incoming packet and local information, the router module determines the direction in which the packet will be forwarded.

• The router contains five direction interfaces, where the local port is used to receive the data generated by the sensor itself, the other direction ports are used for the data forwarding.

• Considering the density of signal lines on PCB, serial communication protocol is used between each routers of the network.

• In order to facilitate the chip test, the debug module is added to the router prototype chip. The main function of the debug module is to generate the test data packet based on the configuration of SPI.