A 60μm2 HV-CMOS pixel with 0.5 ns timing resolution and 28 μW power consumption for high-density arrays

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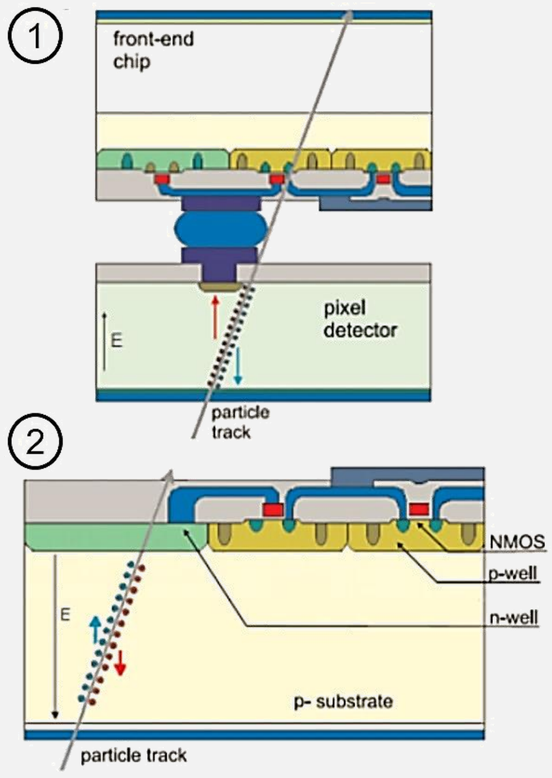
CMOS Active Pixel Sensors



1: Hybrid pixel detector
2: Monolithic Active Pixel Sensor

CMOS Active Pixel Sensors have been used for detection, tracking and vertexing of short-lived particles in High Energy Physics (HEP) experiments.

Hybrid Pixel Detectors

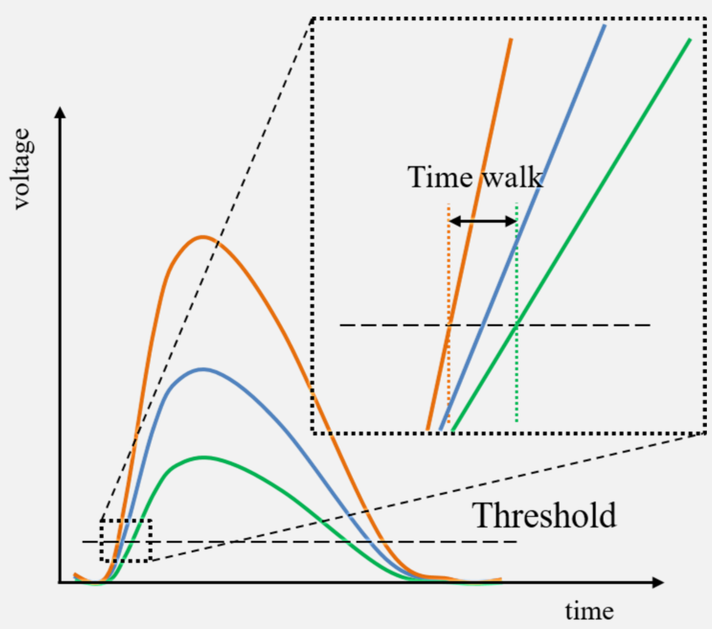
- High radiation tolerance (2x10^{16} n_{eq}/cm^2) and capable to cope with high data rates.
- Expensive and complex assembly process (bump-bonding).
- Significantly thickness of the detector (~300 μm)

Monolithic Active Pixel Sensors (MAPS)

- Integration of sensor and the readout (RO) circuitry in a single layer of silicon.
- Reduced cost of fabrication due to CMOS manufacturing.
- The charge collection is produced by slower diffusion. Thin device thickness (~50 μm).

High Voltage-CMOS (HV-CMOS)

- HV-CMOS are Depleted Monolithic Active Pixel Sensors, i.e. MAPS developed in high resistivity substrates, implemented in standard CMOS process.
- The charge collection is performed by electron drift from the highly biased depleted substrate in hundred of picoseconds.
- HV-CMOS detectors are a suitable candidate for timing applications due to high data rate collection, such in the development of 4D tracking silicon detectors.



Time walk representation on signals of different energies

The time resolution is limited by the charge collection time of the sensor and the response time of the readout electronics ▸▸ Time Walk (TW), i.e. the detection delay of a particle.

Pixel architecture

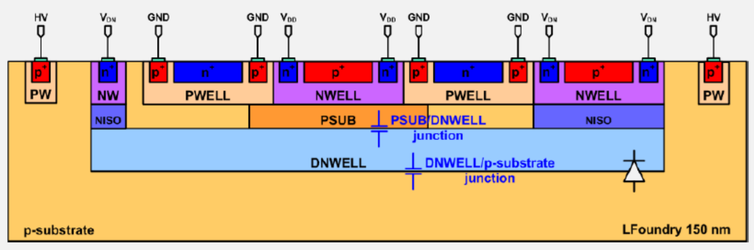
Detector: Diode + Analog RO

→ The deep n-well is used to isolate p-wells from the substrate. The electronics is located in the upper wells. The in-pixel analog readout electronics consists of a sensor bias circuit, a Charge Sensitive Amplifier (CSA), a single folded cascode amplifier, a source-follower and a comparator with a 4-bit DAC for offset compensation.

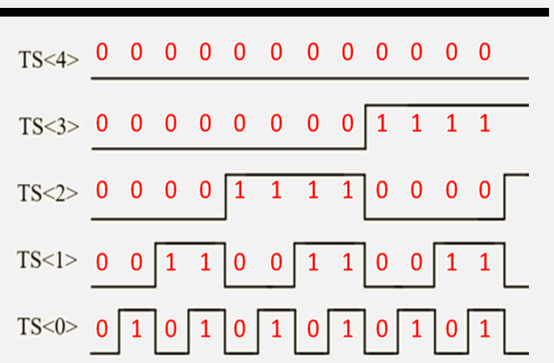
→ The HV-CMOS pixel is designed in the 150 nm process of LFoundry.

Time-Stamp

→ The time-stamp (TS) is saved in several dynamic memories that store the time-stamp. Each pixel receives the TS encoded by an 8-bit Gray code running at 40 MHz.



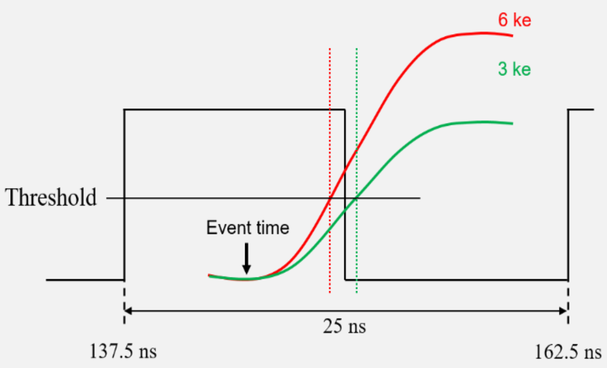
Cross-section of the HV-CMOS pixel



Timing diagram of the time-stamp bits. For simplicity, only the 5 Less Significant Bit are shown

Methods for time resolution enhancement

1. Analog Sampling (AS)



Detection of the hit time for different energies at the edge of the clock

Description

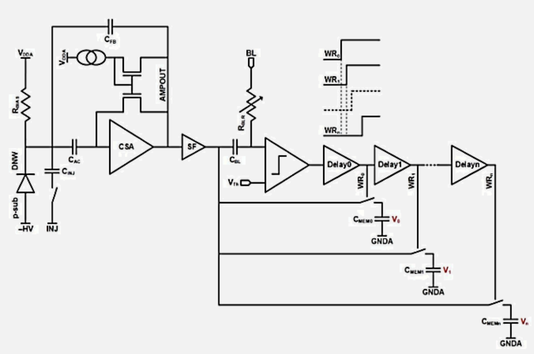
- Low-power method based on storing several analog values of the rising edge of the signal.
- The hit time of the particle is found when the lines obtained from linear regression intersect with the baseline.

Time Resolution

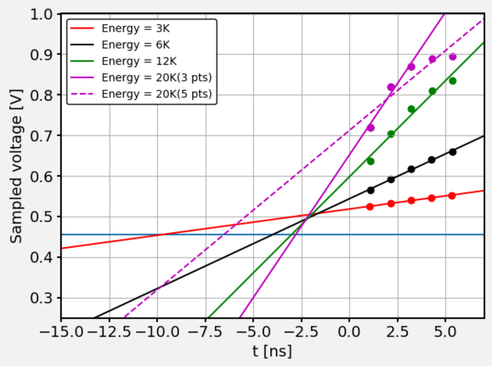
- Below the timing window width (12.5 ns).

Power Consumption

- 17.72 μW for 3 ke$^-$.

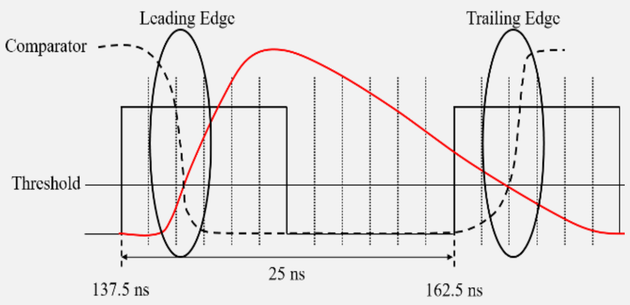


Pixel readout for the analog sampling method



Linear fits of the rising edge of the signals

2. Time-to-digital converter



Representation of the Time-Over-Threshold (ToT)

Description

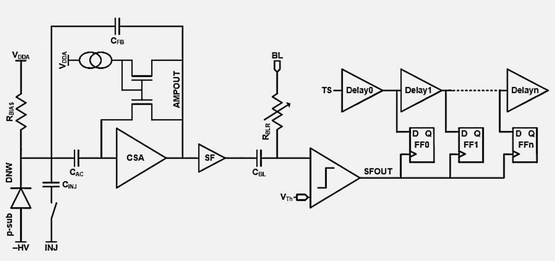
- Method designed to reduce as much as possible the timing window to increase the accuracy in the time of arrival of the particle.
- With the ToT information, the energy of the particle can be calculated off-chip.

Time Resolution

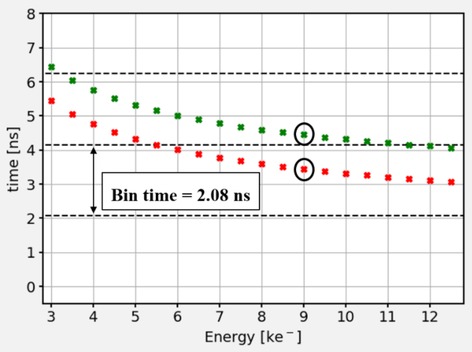
- Below the timing window width formed by 5 bins of 2.08 ns resolution. The TW is reduced, but the bin does not match with the hit time in all cases.

Power Consumption

- 25 μW for 3 ke$^-$.

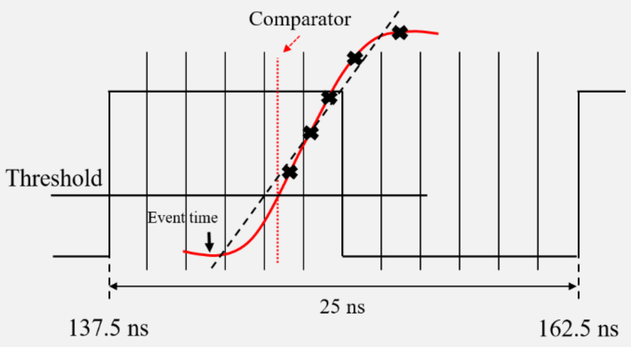


Pixel readout modified for the TDC method



Time-stamp for different signal heights and particle detection times

3. TDC with AS correction



Representation of the method based on the AS + TDC

Description

- This method **combines** the **analog sampling** of the rising edge of the signal and accurate timing by using a **TDC**.

Time Resolution

- Below the timing window width (2.08 ns).
- An off-chip correction based on the linear fit of the signal allows the correct selection of the bin.

Power Consumption

- 28 μW for 3 ke$^-$.

Conclusions: Integration of analog and digital RO electronics in the sensing area of 60 μm x 60 μm HV-CMOS pixels requires a simple and low power design. Compared to similar pixel area detectors, we were able to improve the time walk down to 0.5 ns. The decrease of the TW and the increase of time resolution is reached as a result of an increment in the power consumption, by combining the digital and the analog methods presented.

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