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Design and test of current DACs for threshold tuning of front-end channels for the High Luminosity LHC

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This work is concerned with the design and the characterization of digital-to-analog current converters, developed in a 65 nm CMOS technology, conceived for threshold tuning of front-end channels at the HL-LHC experiment upgrades.
Two DAC structures were integrated in a small prototype chip, that was submitted in August 2018 in the framework of the RD53 developments. The prototype has been tested before and after exposure to X-rays up to a TID of 460 Mrad(SiO_2).
The main performance parameters of the two structures will be compared and discussed in the conference paper.

Summary

Pixel readout chips at the High-Luminosity LHC will deal with extremely high particle rates in a severe radiation environment. In the phase 2 upgrade, the innermost layers of the ATLAS and CMS tracker detectors will be equipped with readout chips that are required to operate with very low stable threshold (of the order of 1000 electrons), with a per-pixel noise occupancy not exceeding 10ˆ-6. In order to achieve this goal, it is vital that the analog front-end features excellent performance from the standpoint of noise and threshold dispersion. Moreover, such performance has to be retained after exposure to total ionizing doses (TIDs) of the order of 500 Mrad(SiO2). Threshold non-uniformities in a multi-channel readout system can be addressed by means of threshold tuning, a procedure during which the threshold of each pixel is locally adjusted with an in-pixel digital-to-analog converter (DAC).
The CERN RD53 collaboration was founded in 2013 to investigate new technologies and architectures for future readout chips. RD53 identified the 65 nm CMOS technology as the candidate process for the development of mixed-signal integrated circuits for the new generation of tracking systems based on high granularity silicon pixels. This technology features the good degree of tolerance to ionizing radiation that is typical of CMOS processes in the 100 nm regime and enables the integration of advanced in-pixel analog and digital functions.
In 2017, the collaboration submitted the RD53A chip, a large-scale chip including a matrix of 400 x 192 pixels (with 50um x 50um pitch), embodying three different analog front-end designs, called Synchronous, Linear and Differential.
A prototype chip including two standalone channels of the Linear front-end has been submitted in August 2018 with the aim of comparing two different DAC designs. Both the submitted channels include a charge sensitive amplifier (CSA) with Krummenacher feedback and a threshold discriminator exploited for time-to-digital conversion. One of the channels is equipped with a 4-bit, binary weighted current DAC featuring cascoded current mirrors, whereas the second one includes a more compact, 5-bit current DAC, with the same binary weighted architecture, but with regular current mirrors.
The performance of the two DACs has been evaluated, in terms of output range, integral and differential nonlinearity, before and after the exposure to a total ionizing dose of 460 Mrad(SiO2) of X-rays. A comparison of the performance of the two DACs will be discussed in the conference paper, in view of their operation in the threshold tuning system of a full-size pixel detector readout chip.

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