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Low-power SEE hardening techniques and error rate evaluation in 65nm readout ASICs

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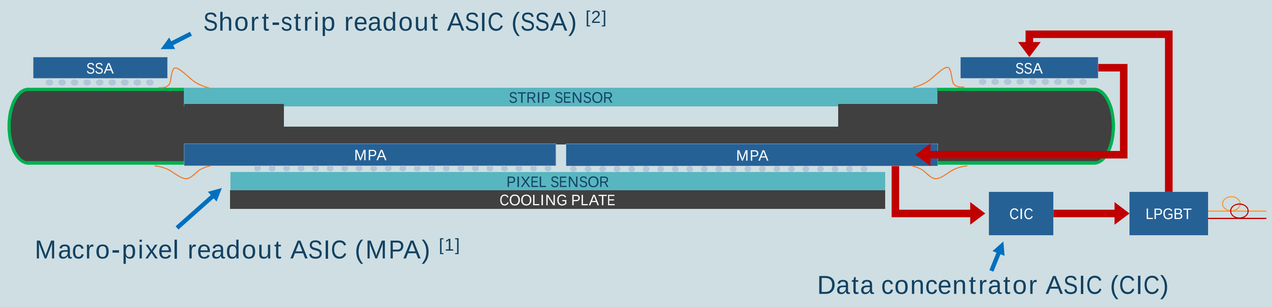
Single Event Effects (SEE) represent one of the main concerns for ASICs exposed to ionizing particles in high energy physics applications. Single event hardening techniques are based on redundancy and may introduce significant overhead in power consumption. In applications as the pixel and strip readout-ASICs for the CMS tracker upgrade, the readout front-end and the complex digital logic capable of performing on-chip real-time discrimination of particles based on transverse momentum, are required to operate with a very tight power budget of 100 mW/cm2. This contribution presents the SEE hardening techniques evaluated for the design in relation to power requirements and affordable error rates. It is essential to study how different parts of the design may benefit from different SEE protecting techniques and eventually which percentage of power consumption could be traded to reach higher radiation tolerance.



- Power density < 100 mW/cm^2
- Power consumption < 250 mW per SSA+MPA couple

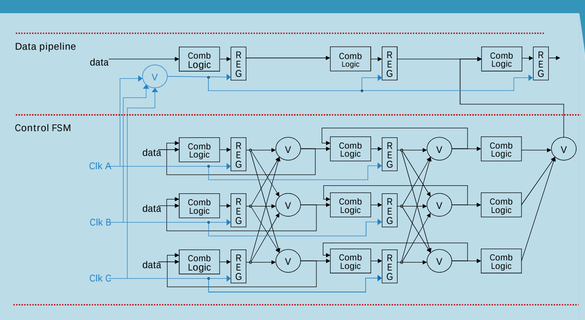
The proposed SEE hardening technique ensures functionality and control reliability while trading a limited data error rate with a minimum power penalty:

SEE HARDENING

At RTL level

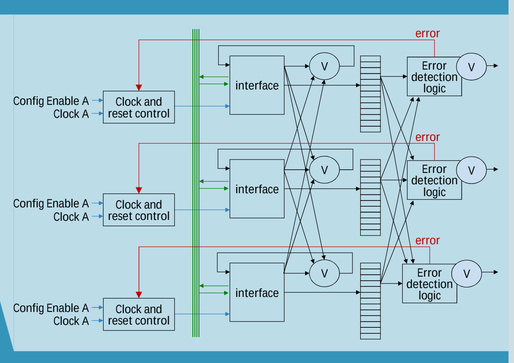
CONTROL AND STATE MACHINES

- Triple module redundancy for SEU protection
- Triplicated clock and reset trees for SET protection
- Voting at each pipeline stage, state variables and outputs signals
- Placement distance >15 µm among registers



CONFIGURATION REGISTERS

- Excluded use of capacitive cells or DICE latches
- Excluded refresh methods (power limitations)
- Triple module redundancy with error detection and self-correction
- Clock enabled only during configuration operations or self-correction



DATA PIPELINE

- No SEU protection applied
- Error rate evaluation via post layout injection simulation

LATCH FIFOS

- Control and header fields triplicated
- Data latches not protected

MEMORIES

- Input latches and decoder with DICE topology
- Memory cell with high input capacitance
- Evaluated the possibility of encoding techniques of forward error correction

SEE SIMULATION

SystemVerilog / UVM environment [3]

SINGLE EVENT EFFECTS EMULATION

- Parse the netlist (gate level or RTL) and extract all registers and nets paths
- Analyse the paths and group the registers and nets by type and by functionality
- Modify cell library model for SEU emulation
- Randomize SEE injection in terms of:
  - Injection path
  - Error probability
  - Uniform distribution for coverage tests
  - SEE time of arrival exponential distribution for error rate evaluation
- Injection of single event effects in multiple ASICs at the same time
- Possibility to focus the SEU injection on subsystem and evaluate the effect at system level

STIMULI GENERATION

- Functionality and the efficiency depends on physics statistics, particle rates and hit occupancy
- Randomized transactions emulating particle detector hits, noise, loppers and jet emulation according the tracker geometry

SEE MEASUREMENTS

With heavy ions on the silicon prototype [4]

SINGLE EVEN EFFECTS MEASUREMENTS

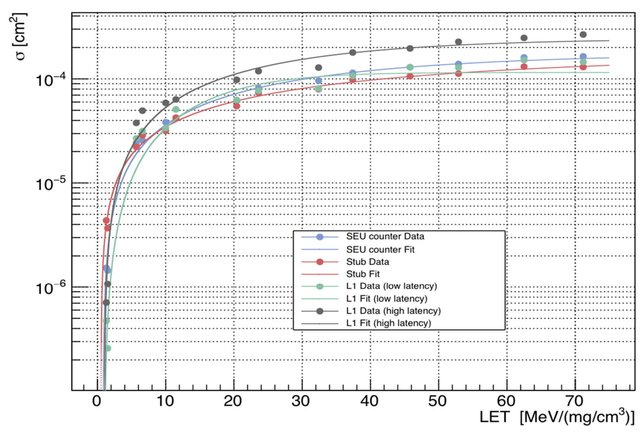
- Test with heavy ion featuring multiple LET allowed to evaluate the SSA cross-section
- While the LET of a pure beam of ions with fixed energy is well defined, the LET of a mixed radiation field is more complex, and the calculation has to be averaged over the different contributing ions
- Experimental SEU cross-section data can be fit with a integral Weibull distribution (as function of deposited ionization energy

$$\sigma = \sigma_0 \left[1 - e^{-\left(\frac{E_{dep} - E_0}{W}\right)^S}\right]$$

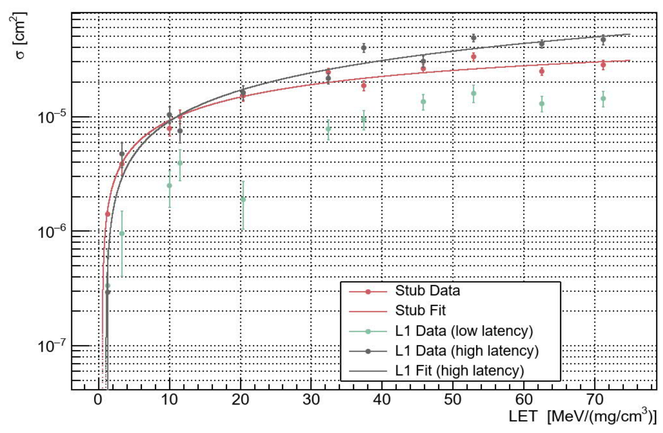
- The cross-section for a specific particle and energy Σ can be approximated as the convolution of the Weibull distribution and the energy deposition probability.
- It can be extended in the case of a radiation environment composed of multiple particle types taking into consideration hadron with energy higher than 20 MeV in the CMS tracker region for 13 TeV p-p collisions, per unit of flux.
- Knowing the ASIC cross-section and the particle spectrum and fluxes, it is possible to approximate the expected error rate in the target application.

CROSSECTION MEASUREMENTS

MPA ASIC MEASURED CROSSECTION



SSA ASIC MEASURED CROSSECTION



EVALUATED CROSSECTION IN THE CMS OUTER-TRACKER REGION for a 13 TeV p-p collisions

	SEU Counter	Stub information	Triggered readout (1 µs latency)	Triggered readout (12.6 µs latency)
MPA	$6.77 \cdot 10^{-11}$ cm^2	$7.92 \cdot 10^{-11}$ cm^2	$5.59 \cdot 10^{-11}$ cm^2	$9.55 \cdot 10^{-11}$ cm^2
SSA	$6.52 \cdot 10^{-11}$ cm^2	$2.74 \cdot 10^{-11}$ cm^2	$0.82 \cdot 10^{-11}$ cm^2	$1.39 \cdot 10^{-11}$ cm^2

ERROR RATE EVALUATION

For a PS Module located at r=21cm, z=265cm from the nominal interaction point (worst case)

	Unit	MPA	SSA	PS Module
Stub information	Per second [s^{-1}]	$1.32 \cdot 10^{-03}$	$4.58 \cdot 10^{-03}$	$< 2.5 \cdot 10^{-03}$
	Per event [BX^{-1}]	$3.31 \cdot 10^{-11}$	$1.14 \cdot 10^{-11}$	$< 6.3 \cdot 10^{-11}$
	Total*	$1.06 \cdot 10^{+05}$	$3.66 \cdot 10^{+05}$	$< 2.0 \cdot 10^{+05}$
Triggered data readout	Per second [s^{-1}]	$1.59 \cdot 10^{-03}$	$2.32 \cdot 10^{-03}$	$< 2.7 \cdot 10^{-03}$
	Per event [BX^{-1}]	$3.99 \cdot 10^{-11}$	$5.79 \cdot 10^{-11}$	$< 6.8 \cdot 10^{-11}$
	Total*	$1.28 \cdot 10^{+05}$	$1.85 \cdot 10^{+05}$	$< 2.2 \cdot 10^{+05}$

*integrated over the total time necessary to reach an integrated luminosity of $4 \cdot 10^{+3}$ fb^{-1}

CONLUSIONS

- The proposed SEE hardening design techniques protect fully the control logic of the ASIC from functional issues and loss of synchronization.
- The bit error rate on the data path of the ASICs is limited to $6.3 \cdot 10^{-11}$ errors per module per event.
- The overall increase in power consumption is estimated to be below 15%.

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[1] D. Ceresa, A. Caratelli, J. Kaplon, K. Kloukinas, J. Murdzek, and S. Scarfi, “Design and simulation of a 65 nm Macro-Pixel Readout ASIC (MPA) for the Pixel-Strip (PS) module of the CMS Outer Tracker detector at the HL-LHC”, PoS, vol. TWEPP-17, 032. 5 p, 2017. DOI: 10.22323/1.313.0032.
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