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Low-power SEE hardening techniques and error rate evaluation in 65nm readout ASICs

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Single Event Effects represent one of the main challenges for digital designs exposed to ionizing particles in high energy physics detectors. Radiation hardening techniques are based on redundancy, leading to a significant increase in power consumption and area overhead. This contribution will present the SEE hardening techniques adopted in the pixel and strip readout ASICs of the PS-modules for the CMS tracker upgrade in relation to power requirements and error rates. Cross-section measurements on the silicon prototypes and expected error-rates evaluated for the CMS tracker particle flux and spectrum will be presented.

Summary

Single Event Effects (SEE) represent one of the main concerns for ASICs exposed to ionizing particles in high energy physics applications. Single event hardening techniques are based on redundancy and may introduce significant overhead in power consumption. In applications as the pixel and strip readout-ASICs for the CMS tracker upgrade, the readout front-end and the complex digital logic capable of performing on-chip real-time discrimination of particles based on transverse momentum, are required to operate with a very tight power budget of 100 mW/cm². This contribution will present the SEE hardening techniques evaluated for the design in relation to power requirements and affordable error rates. It is essential to study how different parts of the design may benefit from different SEE protecting techniques and eventually which percentage of power consumption could be traded to reach higher radiation tolerance.

The full-size prototypes of the SSA and MPA ASICs incorporating all functionality to operate in the CMS experiment have been prototyped in a 65nm technology. For control state machines, a full triple module redundancy (TMR) architecture with 15μm distance among triplicated registers was selected to prevent the ASICs to operate in unknown states. Single event tolerance in clock-gated logic, as the static configuration, was achieved with self-correcting feedback enabled by an SEU detection circuit. For the data memories, encoding techniques have been evaluated. A SystemVerilog/UVM verification environment allowed to simulate the single event effects on the ASIC functionality.

An heavy-ion irradiation campaign allowed to study the capability of the prototype to auto-correct single event induced errors in control and configuration logic and to evaluate the cross-section as a function of the Linear Energy Transfer (LET). The equivalent error-rate extrapolated for the CMS tracker particle flux and spectrum results in less than 5E-12 errors per bunch crossing per module for the continuous transmission of high transverse momentum particles information and less than 4E-11 errors per bunch crossing per module for the triggered readout of the full pixel and strip sensor data.

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