

A SiPM Readout Front-end with Fast Pulse Generation and Successive-Approximation Register ADC

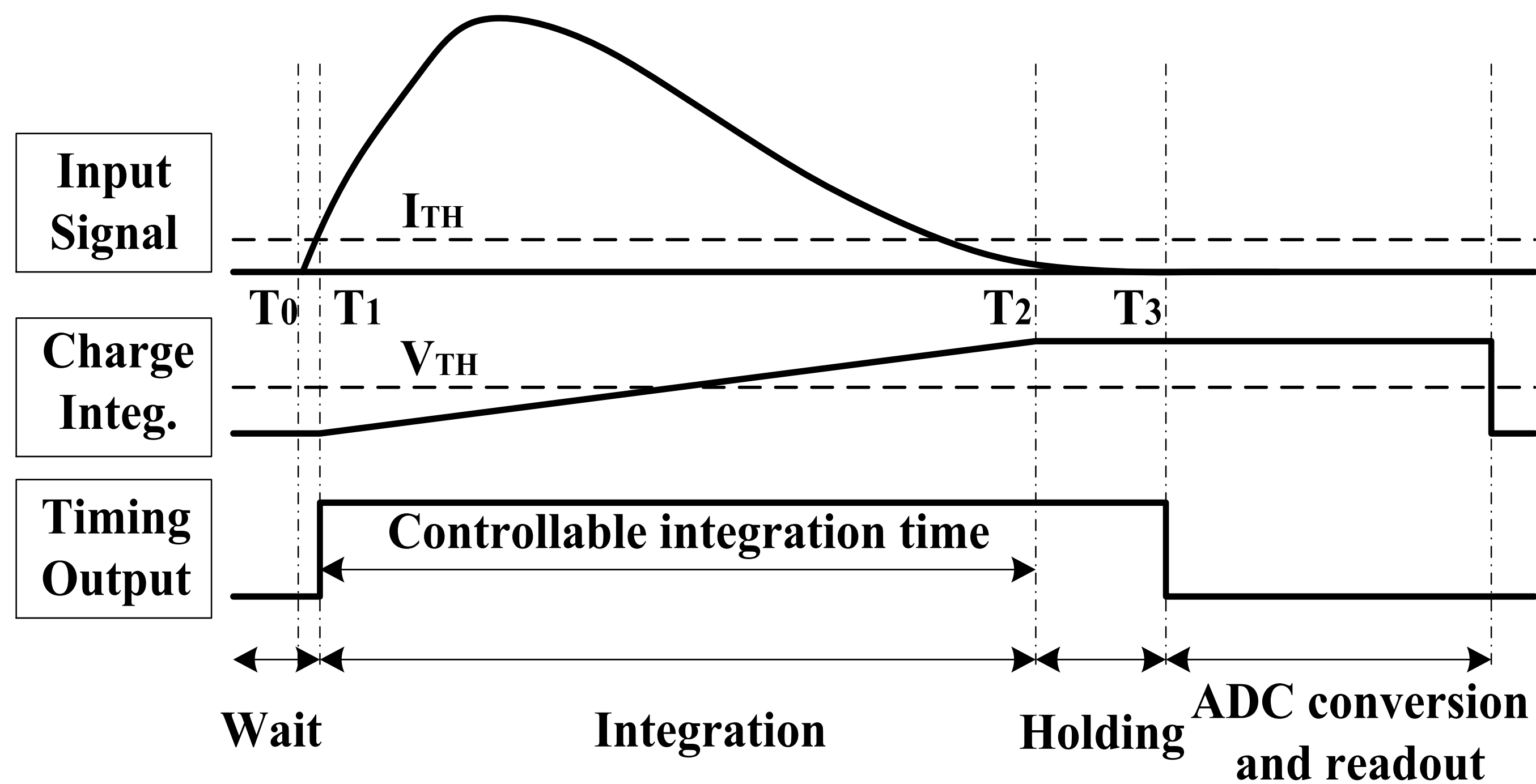
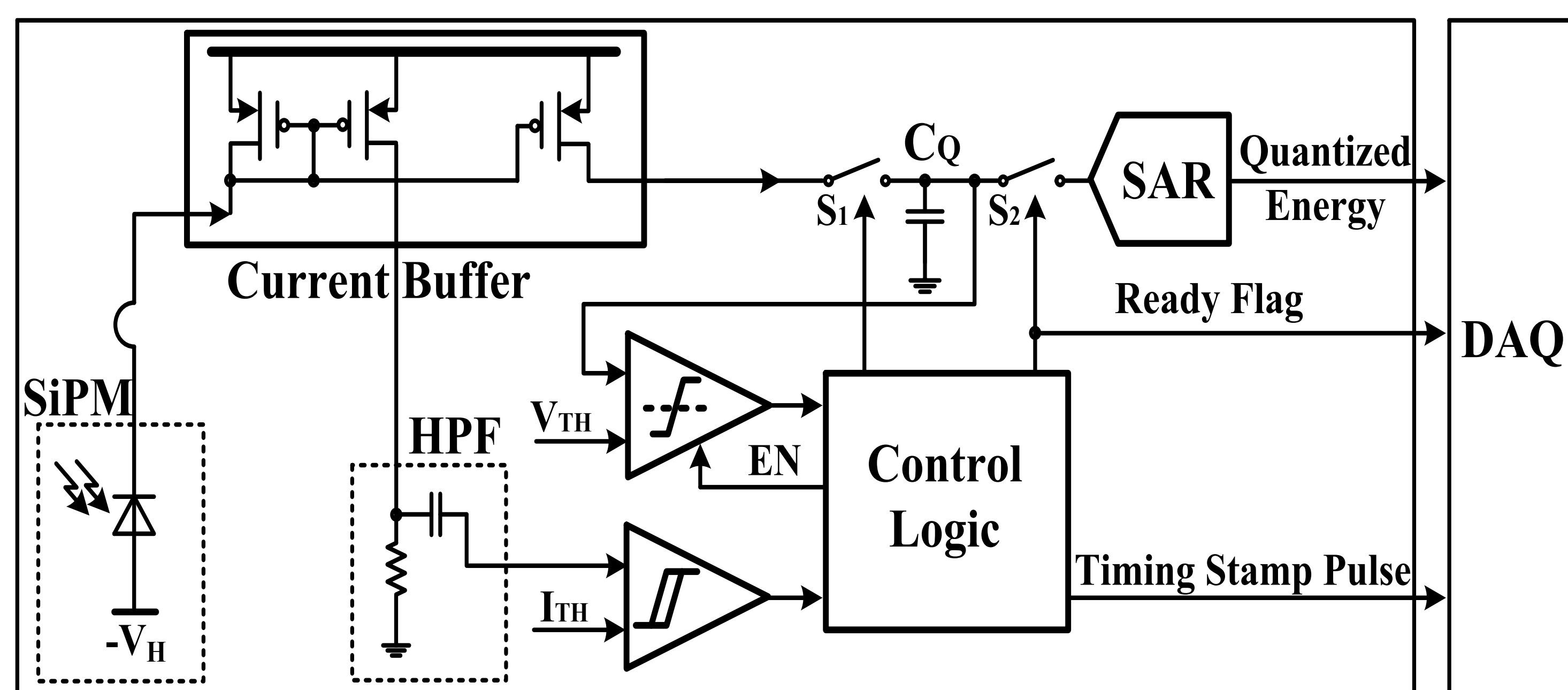
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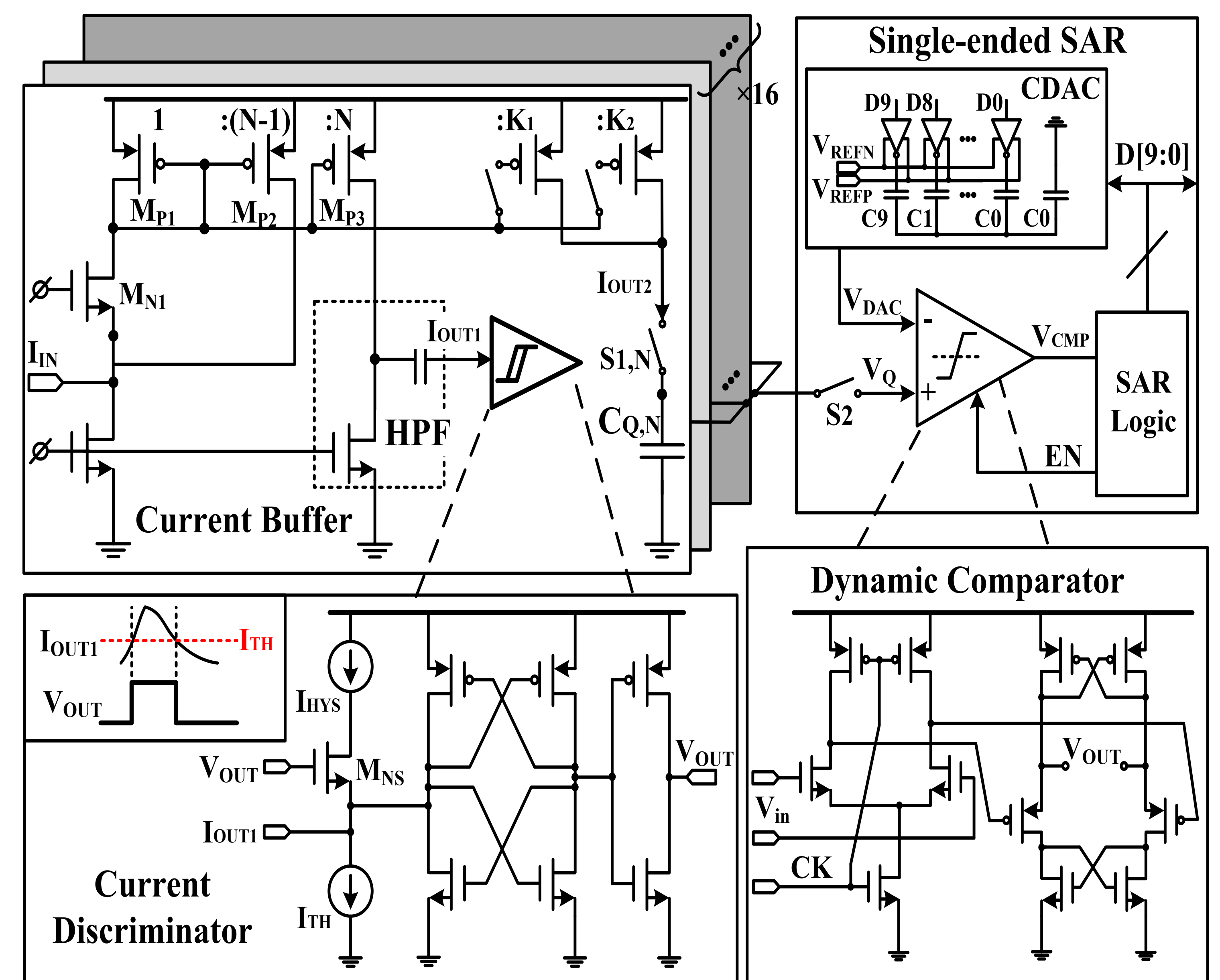
Introduction

- Timing resolution of SiPM readout system is limited by the large quenching RC time constant of SiPM detectors.
- SiPM readouts often have high power consumption due to the power-hungry ADCs and front-end amplifiers.
- This paper presents a low-power high timing resolution 16-channel SiPM readout in 0.18 μm CMOS.
- An on-chip C-R high-pass filter is designed to generate fast pulses for timing improvement without the need of extra I/O pins.
- A single SAR ADC shared among the 16 channels and multiplexed readout is designed to achieve low power consumption.
- A current feedback current buffer structure is developed to reduce the input impedance thus enhancing the input bandwidth.
- The readout system consumes 3.8 mW of power per channel, and the on-chip HPF reduces the long-tailed SPE pulse width from 50 ns to 3 ns.

Architecture and Timing Diagram

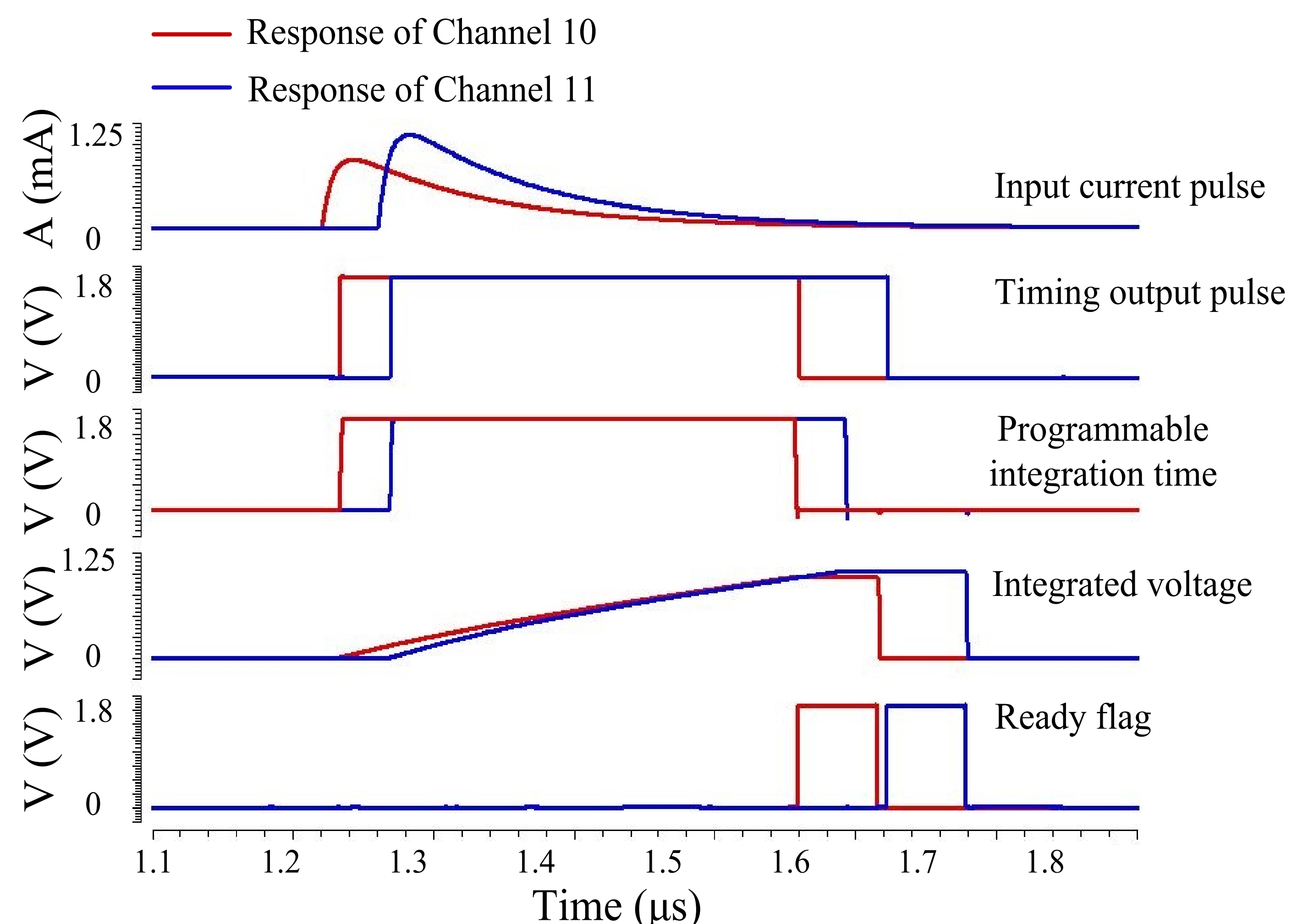


On-chip HPF and Customized SAR ADC



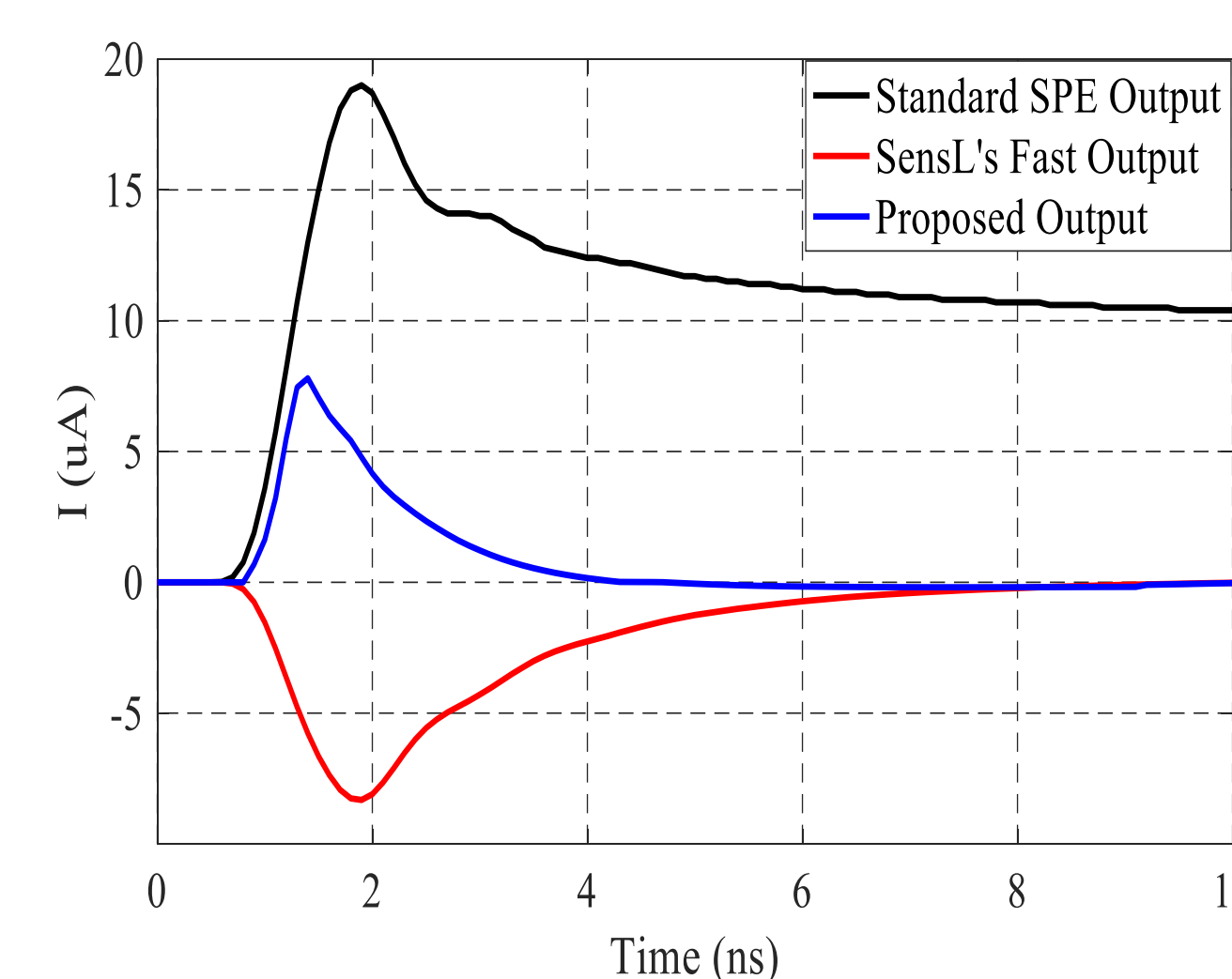
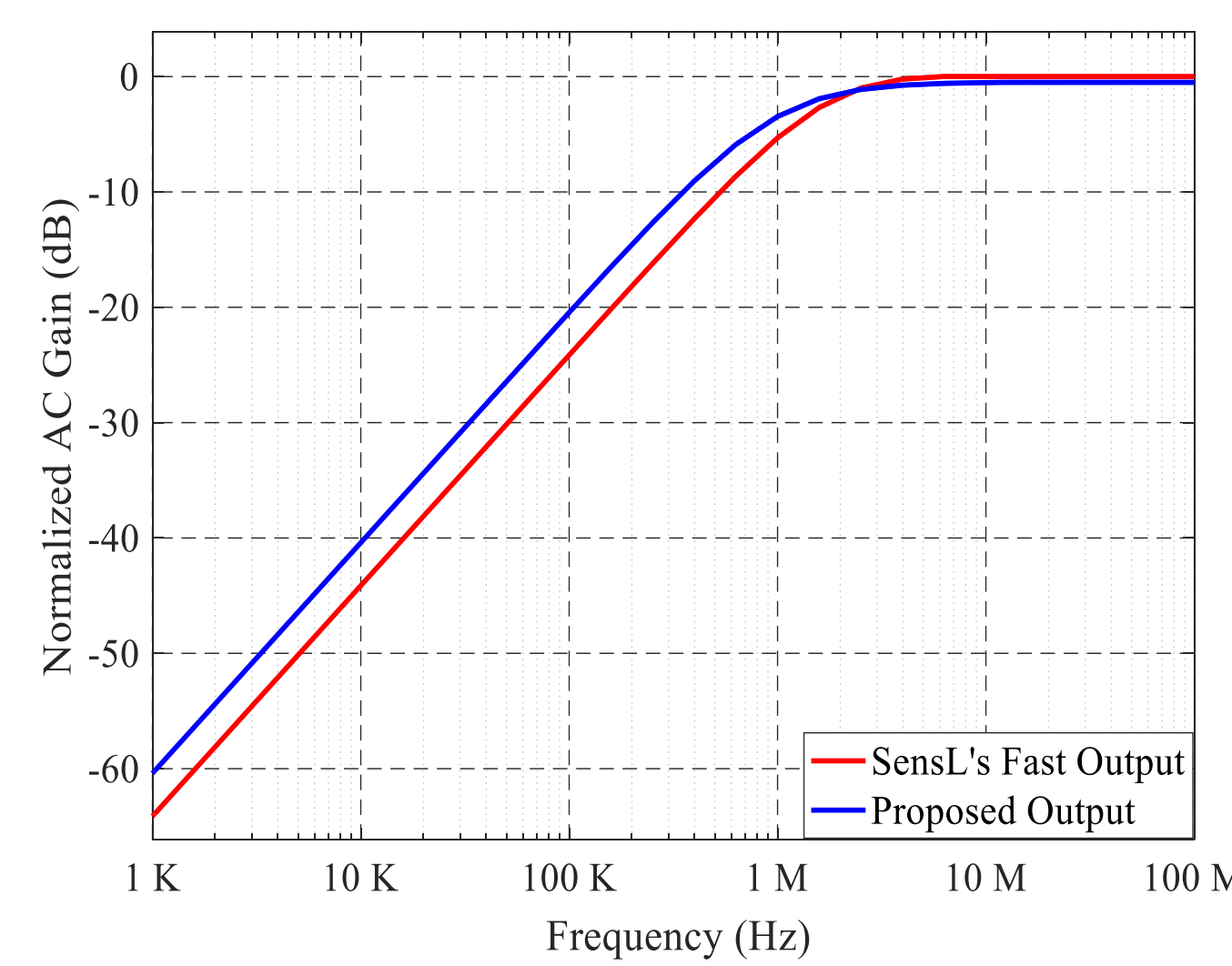
Transient Responses

- Transient responses of two adjacent channels of the proposed SiPM readout are shown below, which are consistent with the timing diagram of the readout.

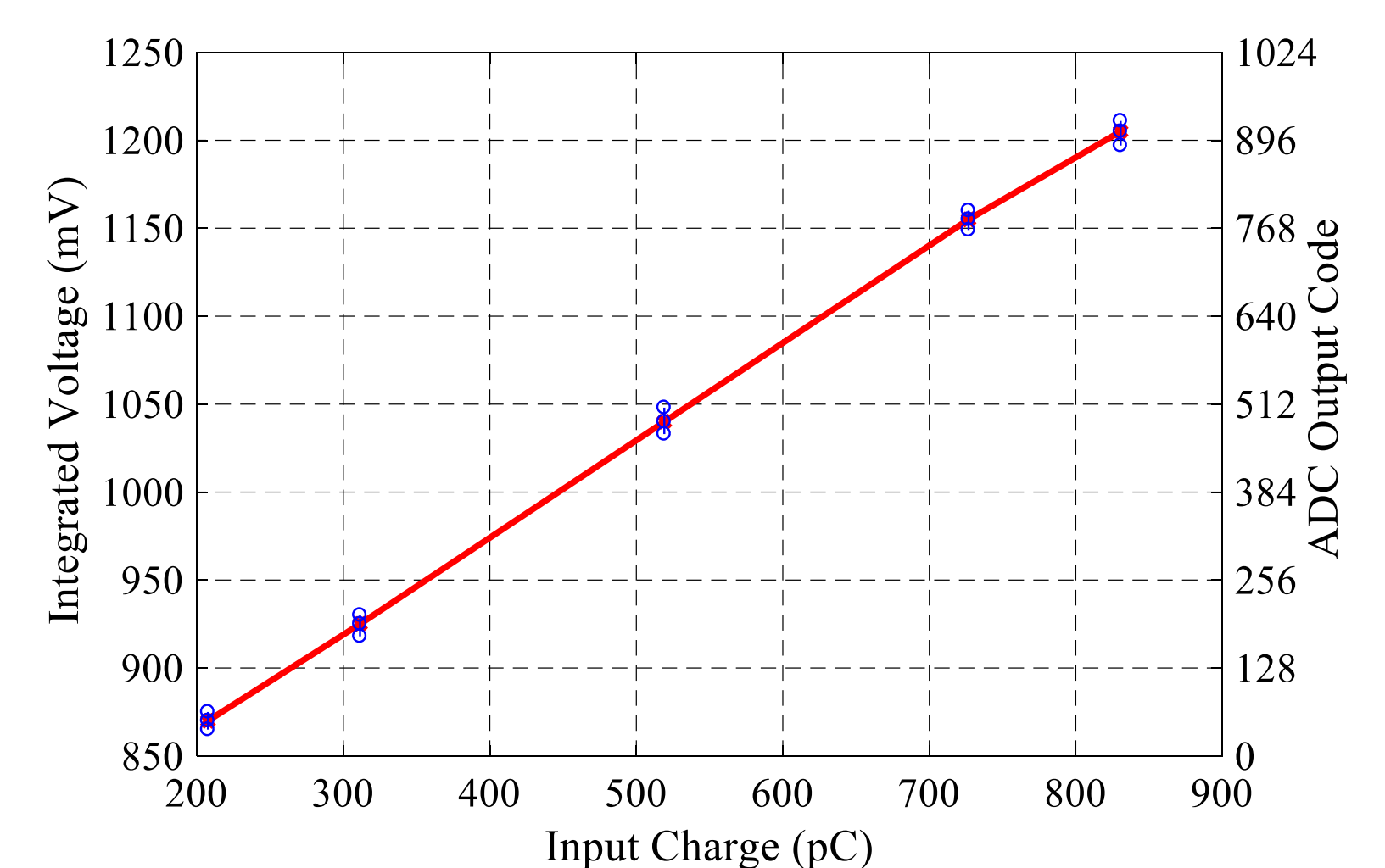
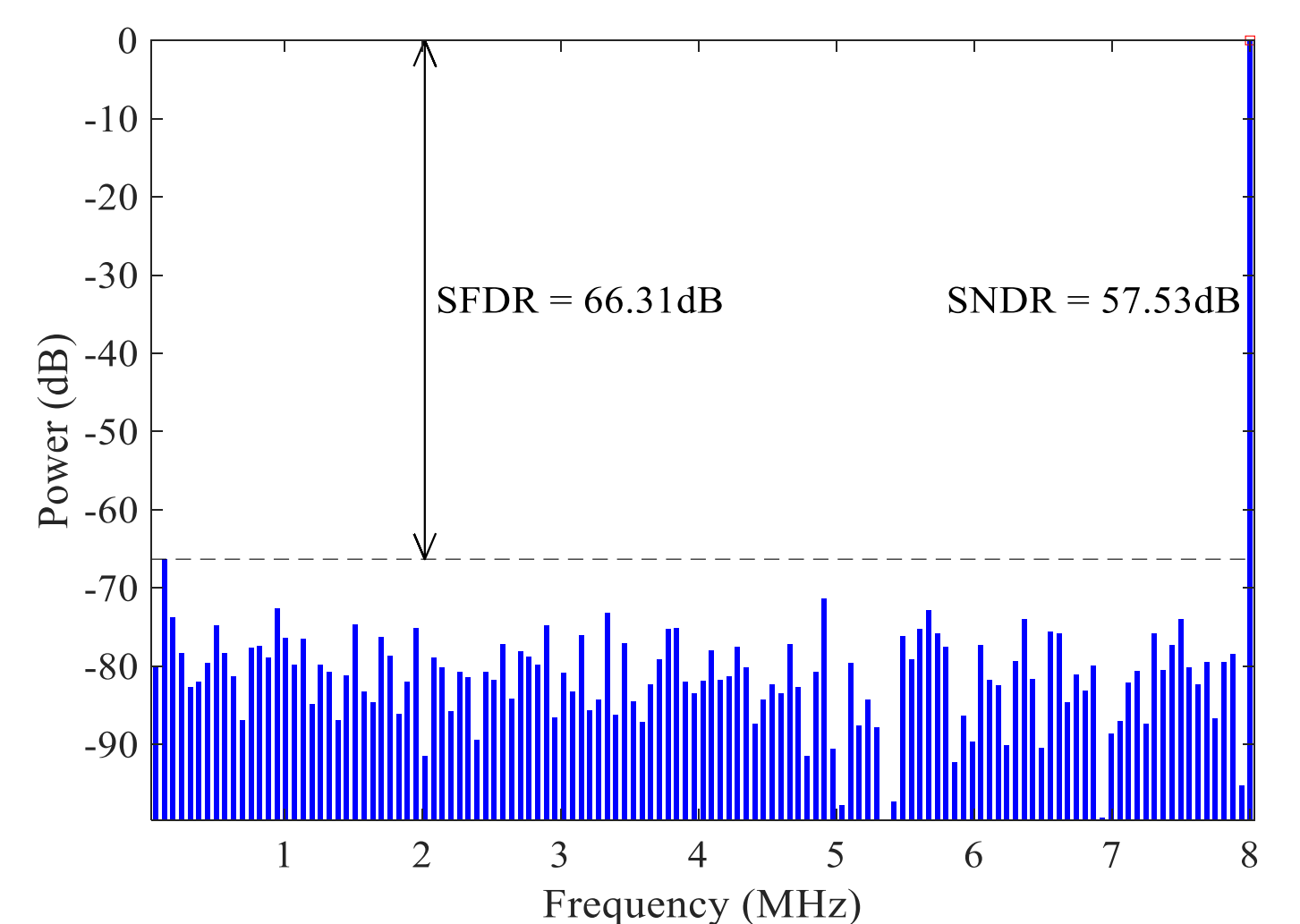


Simulation Results

On-chip HPF



Customized SAR ADC



- The proposed on-chip HPF achieves similar frequency and SPE responses comparing with SensL's SiPM off-chip fast-pulse model.
- By shortening the long-tailed SPE from 50 ns to 3 ns width, a 30 ps timing resolution improvement can be achieved.

- Clocked at 16 MS/s, the proposed single-ended SAR ADC consumes 743 μW from a 1.8 V supply.
- The output spectrum of the ADC with a near-Nyquist input shows a SNDR of 57.53 dB and a SFDR of 66.31 dB, respectively.
- The ADC output codes corresponding to different SiPM charge levels achieves good linearity.