Contribution ID: **156** Type: **Poster**

A SiPM Readout Front-end with Fast Pulse Generation and Successive-Approximation Register ADC

Tuesday 3 September 2019 17:20 (20 minutes)

A low-power front-end with on-chip fast pulse generation and customized SAR ADC is developed for SiPM readout design. The on-chip fast pulse generation improves the timing resolution without the need of extra I/O pins. The proposed SAR ADC, reusing the SiPM charge integrator and eliminating the power-hungry charging sensing amplifier, consumes significantly less power compared with conventional solutions. The front-end is designed in a 0.18 μm CMOS technology, achieving a SNDR of 57.53 dB and consumes 3.8 mW of power. The HPF reduces the long-tailed SPE pulse width from 50 ns to 3 ns.

Summary

ASICs for silicon photomultiplier (SiPM) readout with high timing resolution and low power consumption is required for high-energy physics experiments. However, the large quenching RC time constant of SiPM cause a much longer tail in the single photo-electron (SPE) response. As the output pulse of SiPM is formed by superposition of hundreds of SPE responses from triggered microcells, the current pulse is therefore shaped with a slow rising edge. The slow rising edge of the current pulse makes the timing measurement to be sensitive to the noise of the readout electronics. To address the issue, SensL has developed a modification to the standard SiPM structure that results in a third terminal carrying an ultra-fast output signal. In the modified structure, by adding a small capacitor in parallel with the quenching resistor in each microcell, a high-frequency output path is established from the standard path. Nevertheless, the drawback of the SensL's approach is obvious. As both the fast and standard outputs are required, the input pin counts of the readout ASIC is doubled, which results in a costly and cumbersome design, especially for applications where thousands of SiPM detectors and readout circuitries are needed.

In terms of energy measurement, the conventional SiPM readout ASIC often utilizes a power-hungry charge sensitive amplifier (CSA) to integrate the scaled current onto an integration capacitor, and a low speed Wilkinson ADC is then employed to digitize the CSA output voltage. Such an approach unfortunately suffers from high power consumption. The high power dissipation also inevitably leads to a high working temperature, which can cause SiPMs to generate more dark count noises, deteriorating the timing and energy measurement accuracies. Low-power SiPM readout ASIC is required, especially for systems with a large amount of SiPM detector arrays.

In this paper, we report a 16-channel SiPM readout with high timing resolution, low I/O pin counts and low power consumption. An on-chip high-pass filtering approach is adopted to generate the fast current pulse from the standard output of SiPM without the need of extra I/O pins. The fast current pulse significantly helps to improve the timing measurement accuracy. To achieve low power consumption, a customized SAR ADC directly digitizes the output voltage of the charge integrator in each channel by reusing the charge integration capacitor as the sampling capacitor of the ADC. Besides, benefiting from the high sampling rate of the SAR ADC, the 16 SiPM readout channels can share one single SAR ADC for energy digitization, which offers a compact design and lowers the power consumption of the readout ASIC. Designed in a 0.18 μm 1P6M CMOS process, each channel of the readout consumes 3.8 mW of power. The on-chip HPF shortens the long-tailed SPE pulse width from 50 ns to 3 ns. At 16 MS/s, the SAR ADC consumes 743 μW from a 1.8 V supply, and

provides a SNDR of 57.53 dB and a SFDR of 66.31 dB.

Authors: TANG , Yuxuan (University of Houston); TOWNSEND , Todd (University of Houston); JINGHONG, Chen (University of Houston)

Presenter: TANG , Yuxuan (University of Houston)

Session Classification: Posters

Track Classification: ASIC