Implementation of a RD53A readout chain using FELIX system and the PiLUP board

Nico Giangiacomi
On behalf of the ATLAS TDAQ collaboration

TWEPP CONFERENCE 2019
Overview

**ATLAS Pixel Detector** overview

**Future upgrades**

- **Pixel Detector** Evolution
- **RD53** overview
- **Readout** Evolution

**RD53A-FELIX readout chain**

- Phase-I **FELIX** board overview
- **PiLUP** board overview

**Conclusions and Future developments**
The ATLAS Pixel Detector

The **Pixel Detector** is the innermost sub-detector of the **ATLAS** Experiment and part of the **Tracker** (Inner Detector)

Very **critical** area! Exposed to extremely **high dose of radiation**
The ATLAS Pixel Detector

Fundamental to resolve the primary and secondary vertexes and to reconstruct the tracks


50-350 tracks per bunch crossing [IDTR-2017-007]

$<\mu> \sim 38$
The ATLAS Pixel Detector

Fundamental to **resolve** the **primary** and **secondary vertexes** and to **reconstruct** the tracks

- Sensors very small ➔ **high granularity**
- **Fast** (~10 ns)
- **Low ionization energy** (~3 eV)
- Good signal **proportionality**
- Good resistance to **radiation**
Future upgrades

Phase-I Upgrade (2019-2021)
Many subsystems upgraded (no change for ATLAS ID)

Run-3 (2021-2024)
Higher beam Energy (14 TeV)
300 fb\(^{-1}\) total delivered luminosity
Future upgrades

Phase-I Upgrade (2019-2021)
Many subsystems upgraded (no change for ATLAS ID)

Run-3 (2021-2024)
Higher beam Energy (14 TeV)
300 fb\(^{-1}\) total delivered luminosity

Phase-II Upgrade (2024-2026)
Most ATLAS sub-detectors will be completely redesigned

Run-4 (>2024)
7.5\( \times 10^{34} \) cm\(^{-2} \) s\(^{-1} \) luminosity
3000 fb\(^{-1}\) total delivered luminosity
**ITK, new generation inner detector**

**HL-LHC requirements:**
- Higher **granularity**
- Improved spatial **resolution**
- More **resistant** to radiation

**ITk**
- New **design**
- Only **semiconductor** technology used
- $|\eta| < 4.0$ coverage
- 5 flat pixel barrel layers + 5 pixel inclined layers + 4 strip module layers + 6 end-cap disks
**ITK Pixel Detector**

- Different sensor technologies adopted *(Planar, 3D)*
- Pseudorapidity coverage $|\eta| < 4.0$
- New front-end chip: **RD53**
- Total ionizing dose tolerance $\geq 500$ MRad

New readout **challenge**!

Higher **trigger rate** (100 kHz → 1-4 MHz)
Higher **occupancy** ($<\mu>: 35 \rightarrow 200$)
### ATLAS Pixel Detector evolution

#### B-Layer, Layer 1-2
- Pixel size: **50x400** $\mu^2$
- Active surface: **1.73** m$^2$
- Active surface fraction: **74%**
- Front-end chip: **FEI3 + MCC** (250nm)
- Sensor type: **planar**
- Readout speed: **40-160** Mbps

#### IBL
- Pixel size: **50x250** $\mu^2$
- Active surface: **0.15** m$^2$
- Active surface fraction: **89%**
- Front-end chip: **FEI4** (130nm)
- Sensor type: **planar/3D**
- Readout speed: **160** Mbps

#### ITk Pixel
- Pixel size: **50x50** $\mu^2$
- Front-end chip: **RD53** (65 nm)
- Sensor type: **planar/3D**
- Readout speed: **5.12** Gbps
RD53A, the ITk Pixel FE prototype

- Pixel size: 50x50 μ²
- Pixel matrix: 192x400 pixels
- Realized with 65 nm technology
- Sensor type: planar/3D
- Readout speed: 5.12 Gbps (4x1.28Gbps)
- Output Encoding: Aurora 64/66b
- Can be constantly reconfigured during data-taking
- Design technology: Analog island on Digital “sea”
- Bonded on Single Chip Card (SCC) test chip
- SCC interface: Display Port + JTAG

https://www.xilinx.com/support/documentation/ip_documentation/aurora_64b66b_protocol_spec_sp011.pdf
The FELIX readout system

FELIX → off-detector readout system common to all the sub-detectors

Will replace the current ATLAS custom-made off-detector cards (RODs) during 2019-21 Phase-I upgrade (partially) and during 2024-24 Phase-II upgrade (completely)

Phase-II hardware design still under investigation

Phase-I cards under production

FELIX project involving several institutes

- (up to) 48 links (optical fibers)
- PCIe gen 3 technology → >100 Gbps
- 7th series Ultrascale Xilinx FPGA

https://atlas-project-felix.web.cern.ch/atlas-project-felix/
RD53A readout demonstrator

**GOAL:** realize a **readout chain for RD53A** prototype using **Phase-I FELIX** and **ITk readout software**

**BUT SCC and FELIX card not directly compatible**

**SCC**
- Connection interface: 4 lanes electrical links (Display Port)
- **Input** from DAQ protocol: 160 Mbps serial
- **Output** to DAQ protocol: Aurora 64/66b

**Phase-I FELIX**
- Connection interface: Optical link ($\leq$1 per FE)
- **Input** from Front-End protocol: GBT/Full Mode
- **Output** to Front-End protocol: GBT

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[https://www.xilinx.com/support/documentation/ip_documentation/aurora_64b66b_protocol_spec_sp011.pdf](https://www.xilinx.com/support/documentation/ip_documentation/aurora_64b66b_protocol_spec_sp011.pdf)
[https://espace.cern.ch/GBT-Project/default.aspx](https://espace.cern.ch/GBT-Project/default.aspx)
[https://edms.cern.ch/document/2160023/1](https://edms.cern.ch/document/2160023/1)
Solution: use Protocol Converter as an interface
PiLUP board overview

PiLUP board developed by INFN and University of Bologna

- Two 7th series Xilinx FPGAs in Master-Slave architecture
- Embedded ARM dual core processor
  - Linux system
- PCIe bus → 32 Gbps
- Highly versatile
  - Several connectors

- Several connectors
  - Ethernet
  - FMC
  - SFP
  - SMA

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Protocol Converter overview

\textbf{πLUP}: system interface  \hspace{2cm} \textbf{FELIX}: main DAQ board  \hspace{2cm} \textbf{Can interface up to 4 SCC chips}

Main blocks:

- **Configuration** (FELIX → RD53A), decodes command from FELIX GBT and encodes them into RD53A compatible format

- **Data reception** (RD53A → FELIX) implemented, decodes Aurora 64/66b from SCC, merges 4 links into a single stream that is encoded into Full_mode protocol

- **Trigger generator** (if no TTC available)

- **RD53A emulator** (optional) implemented into protocol converter
Protocol Converter overview

\(\text{nLUP}:\) system interface

\(\text{FELIX}:\) main DAQ board

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- **RD53A emulator** (optional) implemented into protocol converter

Can interface up to 4 SCC chips
Setup description:

- Server + FELIX card
- Optical fiber(s)
- PiLUP board as Protocol Converter
- DP mezzanine card(s) (two version available: Single Module Adapter and Multi-Module Adapter)
- Display Port cable(s)
- SCC (RD53A)
**Setup overview**

1 PiLUP → 4 SCCs
(4 lanes, 5.12 Gbps)

Setup description:
- Server + FELIX card
- Optical fiber(s)
- PiLUP board as Protocol Converter
- DP mezzanine card(s) (two version available: Single Module Adapter and Multi-Module Adapter)
- Display Port cable(s)
- SCC (RD53A)
Setup overview

1 FELIX (FLX-712) → 48 SCCs
(4 lanes, 5.12 Gbps)

Setup description:
- Server + FELIX card
- Optical fiber(s)
- PiLUP board as Protocol Converter
- DP mezzanine card(s) (two version available: Single Module Adapter and Multi-Module Adapter)
- Display Port cable(s)
- SCC (RD53A)
Results

RD53A – PiLUP – FELIX readout chain realized and fully working

- Up to 4 SCC chips can be interfaced by one PiLUP card
- SCC chips readout at maximum speed (4x1.28 Gbps)
- Readout software integrated with ITk Phase-II software
- Chip calibrations realized → Digital Scans + Analog Scans (see example in figure)
- Current architecture will be used as a baseline for final Phase-II implementation

ANALOG SCAN (example)
ATLAS Pixel Detector fundamental to resolve particle tracks
Pixel Detector upgraded to have more spatial resolution and channel density
Readout system upgraded to face harsher environmental conditions
First prototype (Front-End and readout chain) realized
Real FE chip (RD53B) and Phase-II readout system development still ongoing

Alternative architecture prototypes existing (see backup slides)
THANK YOU
FOR YOUR ATTENTION
BACKUP SLIDES
Alternative RD53A readout

Main Features:

- HDMI cable copper, 160 Mb/s
- Interface card electrical → optical
- RD53A outputs @ 1.28 Gb/s
- MM fiber
- GBT @ 4.8 Gb/s
- FLX 712
- DP cable, copper 160 Mb/s & 1.28 Gb/s
Alternative RD53A readout

Main Features:

- **Interface Card** (designed by ANL) to perform **electro-optical conversion**
- **QFSP**, one optical fiber for Aurora lane (4 lanes per SCC)

Future upgrade planned:

1 Interface Card → 12 SCCs (4 lanes at 1.28 Gbps)
Main Features:

- **Interface Card** (designed by ANL) to perform **electro-optical conversion**
  - QFSP, one optical fiber for Aurora lane (4 lanes per SCC)
  - **VLDB** card for GBT→ elink (downlink)
Alternative RD53A readout

Main Features:

- **Interface Card** (designed by ANL) to perform **electro-optical conversion**
  - QFSP, one optical fiber for Aurora lane (4 lanes per SCC)
  - VLDB card for GBT → elink (downlink)
  - FELIX Firmware “modified”
    - “Aurora 64/66b” decoding
    - Lane merging

**Aurora Latency = 125 ns**

1 Phase-1 FELIX (FLX712) →
Up to 48 SCCs (1 lane, 1.28 Gbps))
Up to 12 SCCs (4 lanes, 5.12 Gbps)
Front-end electronics overview

Front-end readout electronics realized in CMOS technology and bump-bonded to the sensors

Analog Part

- Filters and discriminates signal
- Configurable analog thresholds

Digital Part

- ToT calculation
- Data processing, collection and transmission
- Chip configuration
Pixel Sensor Overview

A pixel sensor is a p-n junction realized with semiconductor materials in inverse polarization regime. Particles create electron-hole couples in the depletion zone.

- Very small $\rightarrow$ high granularity
- Fast (~10 ns)
- Low ionization energy (~3 eV)
- Good signal proportionality
- Good resistance to radiation
Pixel sensors: Planar - 3D - HV-CMOS

PLANAR

metal oxide, p-implant

particle track, back side bias

depletion zone, n-bulk

ohmic n-side contact

3D

HV-CMOS

PMOS, NMOS

deep n-well

deprecated zone

p-substrate
ITk efficiency

ATLAS Simulation

$t\bar{t}$, $p_T > 1$ GeV, $\sqrt{s} = 14$ TeV

Track Reconstruction Efficiency

$\langle \eta_{vertices} \rangle$

ATLAS Simulation

$t\bar{t}$, $p_T > 1$ GeV, $\sqrt{s} = 14$ TeV

ITk, $\langle \mu \rangle = 200$

Run-2

Linear Fit ($\mu = 40 - 100$)

Run-2 - $\mu = 40 - 80$
ATLAS TDAQ evolution

Phase-0

- Custom Front-End chips
- Custom Readout off-detector boards (RODs) specific to each Front-End
- Common ROD interface (ROS)
- Commercial PCs for High Level Trigger (HLT)
ATLAS TDAQ evolution

Phase-I (2019-2023)

- Custom Front-End chips
- Hybrid off-detector Readout system: custom boards specific to each Front-End + common interface for multiple Front-Ends (FELIX)
- Commercial PCs for High Level Trigger (HLT)

* GBT: GigaBit Transceiver with Versatile Link

05/09/2019
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ATLAS TDAQ evolution

Phase-II (> 2024)

- Custom Front-End chips
- Common off-detector Readout boards for all the Front-Ends (FELIX)
- Commercial PCs for High Level Trigger (HLT)

*LPGBT: Low power GBT*
DP Mezzanine

Single Module Adapter (SMA)
- Only FMC HPC compatible
- 1 DP connector
  - 4 lanes GTX Rx
  - 1 lane IO (elink)
- 1 DP connector
  - 5 lanes IO

Multi Module Adapter (MMA)
- FMC HPC and LPC compatible
- 4 DP connectors
  - 4 lanes IO
  - 1 lane IO (elink)