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Implementation of a RD53A readout chain using FELIX system and the PiLUP board

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RD53A is the first prototype of RD53, the pixel detector front-end chip that will be used by the ATLAS and CMS experiments at CERN during HL-LHC, starting operation in 2026. It is implemented using 65 nm technology and it transmits data using up to four lanes running at 1.28 Gbps each. This presentation will describe the implementation of a first readout chain of the RD53A using the ATLAS FELIX card. The readout chain features a third card, called PiLUP, as a protocol converter between RD53A and FELIX, with direct communication planned in future revisions.

Summary

To improve physics reach and overcome the challenge of the increasing luminosity of High Luminosity LHC (HL-LHC), the ATLAS experiment will undergo a major upgrade programme. For the Pixel Detector there are three key factors required: the increase of spatial resolution, the ability to withstand a very high radiation dose and to transmit at high bandwidth. A research programme aimed at fulfilling all the aforementioned requirements led to the development of RD53, a pixel detector front-end chip realized using 65 nm CMOS technology. While the final implementation of the chip has not been completed a first prototype, called RD53A, has been produced and is currently being tested.

To maximize chip testing efficiency and to drive development of the Data AcQuisition (DAQ) chain to be used by ATLAS at HL-LHC, it is extremely important that, even for the first prototypes, the DAQ chain is as similar as possible to the final intended design. For the ATLAS experiment, the HL-LHC readout chain will be implemented using the Front-End LInk eXchange (FELIX) card as the first layer of off-detector electronics. This presentation describes the implementation of a first DAQ structure for the RD53A chip using the FELIX system. At this early stage, the FELIX and RD53A cannot be interfaced directly. The currently FELIX implementation, aimed in the first instance at upgrades to be installed earlier than HL-LHC, communicates via optical fibers through either a 4.6 Gbps GBT protocol or a custom 9.8 Gbps protocol known as FULLl Mode protocols. RD53A communicates via Display Port (DP) connectors through 160 Mbps GBT E-link (input) and four lanes 1.28 Gbps Aurora 64/66 protocol (output).

In order to bridge the two systems for the purposes of the demonstrator another board, called PIxel detector high Luminosity UPgrade (PiLUP), is therefore used in the chain. The PiLUP handles both the FELIX-to-RD53A data-path (downlink) and the RD53A-to-FELIX path (uplink). This is done through different firmware blocks: the GBT_FPGA block, the TTC_Encoder, the Aurora Decoder, the Protocol Converter block and the Full_Mode encoder. The GBT FPGA block decodes the GBT-formatted data from FELIX, containing the configuration commands for the RD53A chip, and also synchronizes to the FELIX clock, recovering it from the data-stream. Both configuration commands and clock are then propagated to the TTC Encoder firmware block, which is in charge of converting the commands to a RD53A compatible format and of encapsulating them in a single 160 Mbps serial line, connected to one of the DP connector data lanes. Concurrently the PiLUP receives and decodes Aurora 64/66 data from the RD53A chip, coming from the other four data lanes of the DP connector. Those four lanes of 1.28 Gbps data (resulting in a total throughput of 5.12 Gbps) are then passed to the Protocol Converter firmware block, which merges them into a single FULL Mode stream that is transmitted to Felix via optical connection.

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