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Development of the Compact Processing Module for the ATLAS Tile Calorimeter Phase-II Upgrad

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The LHC Phase II Upgrade of the ATLAS Tile Calorimeter (TileCal) implies a new readout and trigger architecture. The on-detector readout electronics will transmit detector data to 32 Tile PreProcessor (TilePPr) boards in the counting rooms at the LHC frequency, sending selected data to the ATLAS FELIX and interface with the trigger systems. Each TilePPr is composed of four Compact Processing Modules (CPM) with single-width AMC form factor and one full-size ATCA carrier with 4 slots. This contribution presents the design of the CPMs and first experiences, and reviews the results of the TilePPr prototype for the TileCal Demonstrator programme

Summary

The Tile Calorimeter (TileCal) is one of the subdetectors composing the ATLAS detector at the Large Hadron Collider (LHC). The LHC Phase II Upgrade of TileCal includes the complete redesign of the on- and off-detector electronics, and the implementation of a new readout architecture with new interfaces to the upgraded full digital trigger system.

After the Phase II upgrade, the on-detector readout electronics will transmit the detector data to the Tile PreProcessor (TilePPr) boards in the counting rooms for every bunch crossing (every 25 ns), leading into required data bandwidth of ˜40 Tbps to read out the entire detector. The TilePPr board will store the digitized samples in pileline memories until the reception of a trigger acceptance signal when the data will be transmitted to the Front End LInk eXchange (FELIX) system. The data received from the detector is processed in real-time and calibrated energy and time per cell for every bunch crossing are transferred to the first level of trigger through the Trigger and DAQ interface system (TDAQi).

Each TilePPr module will read out and operate eight TileCal modules, requiring a total of 32 TilePPr modules for the complete readout and operation of the detector. Each TilePPr comprises four Compact Processing Modules (CPM) with single-width Advanced Mezzanine Card (AMC) form factor, one full-size Advanced Telecommunications Computing Architecture (ATCA) carrier with 4 slots, and one GbE switch and one ARM-based computer mezzanine cards. The high-speed communication with the on-detector electronics, data acquisition and core processing functionalities relies on the CPMs, while functionalities for power management, control and configuration of the TilePPr boards are implemented in the mezzanine cards.

Each single AMC CPM hosts eight Samtec FireFly modules with MXC connectors; a Xilinx Kintex UltraScale FPGA for data buffering, digital processing and control; a Xilinx Artix 7 FPGA for slow control and monitoring; and high-speed interconnections to communicate with the TDAQi through the Zone 3 connector. The CPMs provides a high-speed path with the on-detector electronics through 32 GigaBit Transceiver (GBT) links running at 4.8 Gbps for the downlink (to the on-detector electronics) and 9.6 Gbps for the uplink (from the on-detector electronics) with fixed and deterministic latency.

The CPM design is based on the TilePPr prototype developed as part of the Demonstrator programme. This board is a double mid-size AMC form factor equipped one Xilinx Virtex 7 FPGA to read out the Demonstrator module and one Kintex 7 FPGA to perform trigger to perform preprocessing tasks. The TilePPr prototype has served to evaluate the new readout architecture with a fully functional prototype of the upgraded on-detector electronics during six test beam campaigns at the SPS accelerator facilities between 2015 and 2018.

This contribution presents in detail the design and integration plans of the Compact Processing Modules for the ATLAS Tile Calorimeter Phase II Upgrade, as well as, the results and experiences with the designed prototypes for the TileCal Demonstrator programme.

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