Highly-linear FPGA-based Data Acquisition System for Multi-channel SiPM Readout

Todd Townsend, Yuxuan Tang, Jinghong Chen

Department of Electrical and Computer Engineering,
University of Houston, Houston, TX 77204

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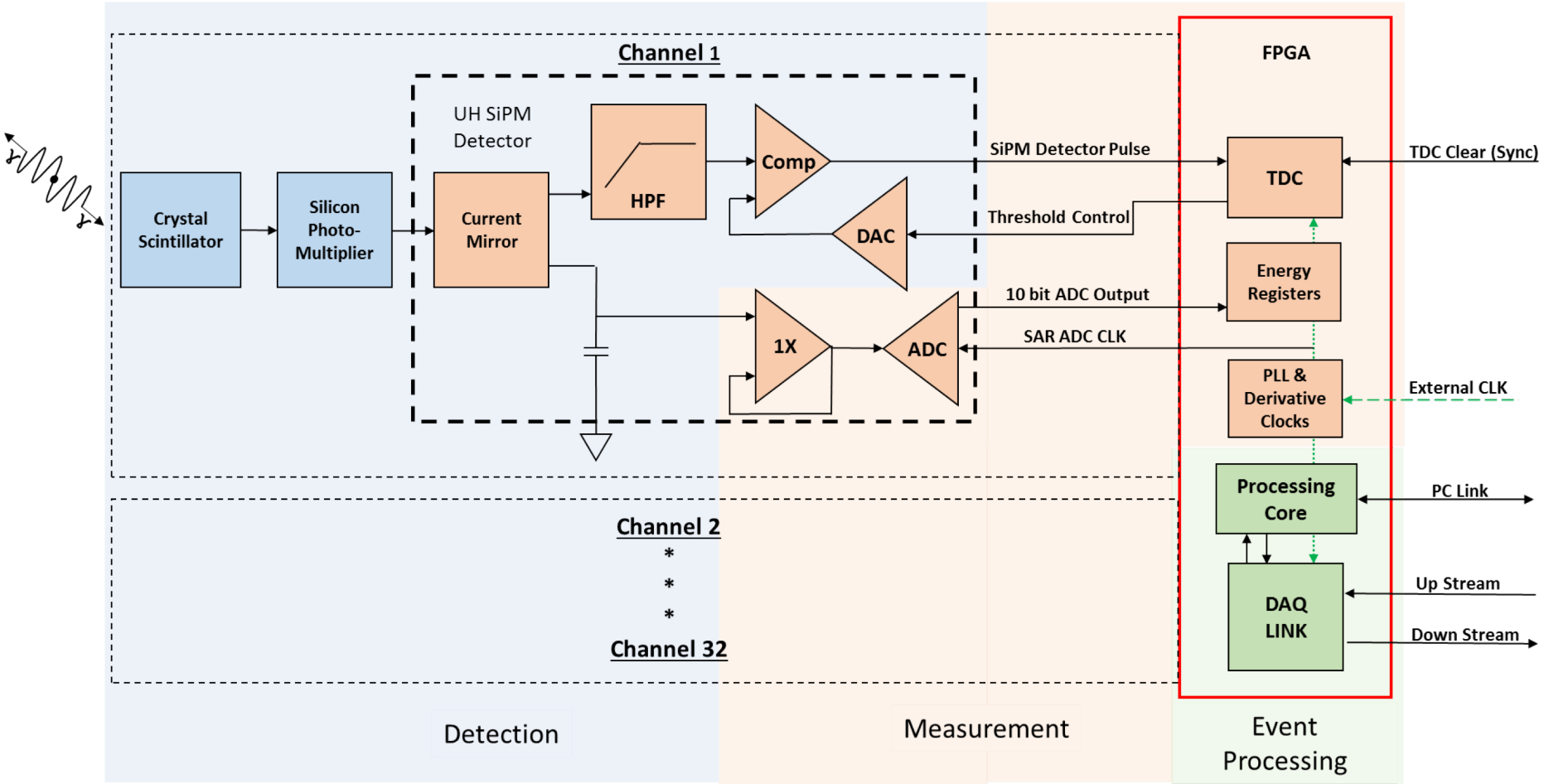
Outline

- Motivation
- SiPM FPGA DAQ Architecture
- Detection
- Pulse Energy
- TDC
- Results
- Summary

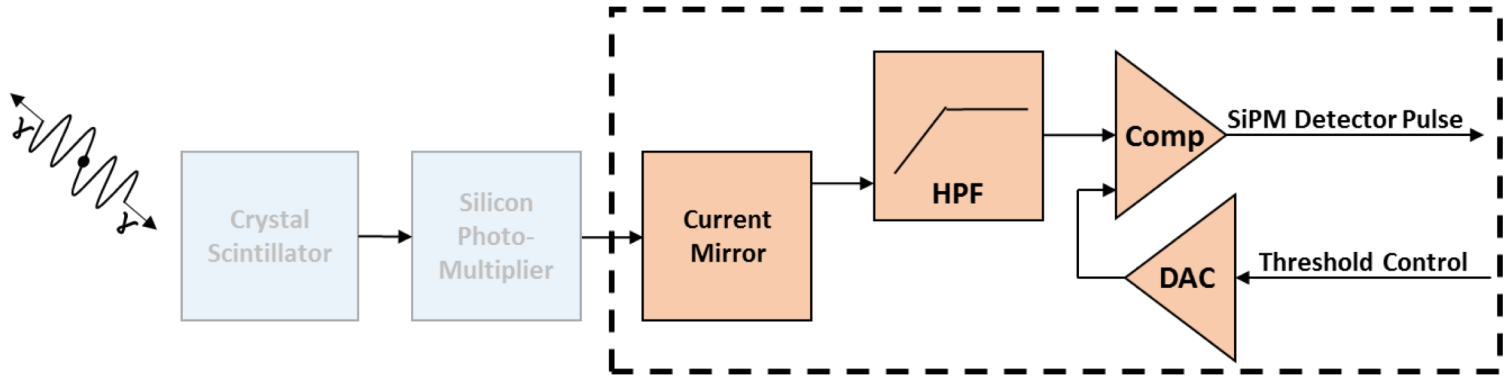
Motivation

- Maximize input channels per FPGA for time-of-flight with energy measurement
- Utilize 28nm Kintex 7 FPGA for best price/performance/watt
- Simplify SiPM pulse energy measurement with interface to new UH designed detector
- Increased linearity

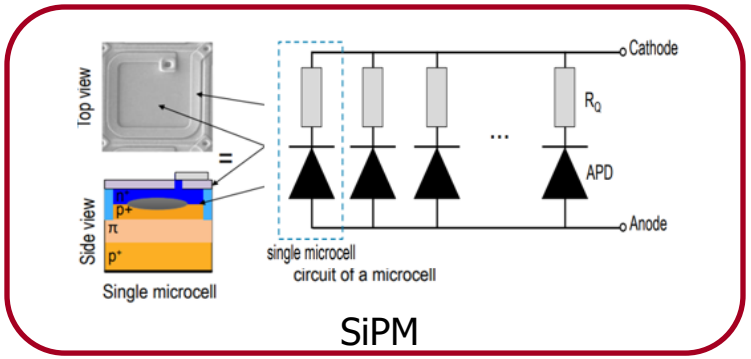
SiPM FPGA-based DAQ



Detection

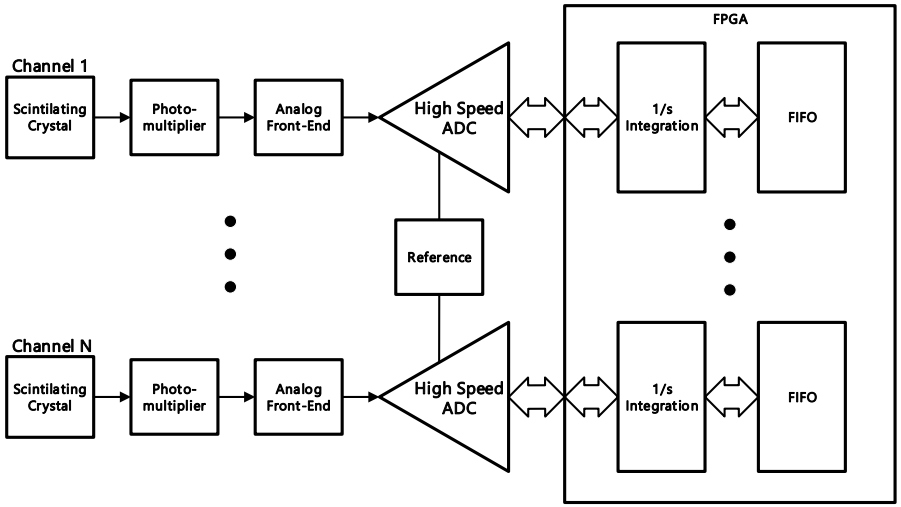


- Selection of the scintillation material determines the gain and decay rate which dictates the full width half maximum TOF possible*
- Photomultipliers can be either a photomultiplying tube (PMT) or silicon based (SiPM)
- As resolution requirements increase, SiPMs are chosen due to their advantage with:
  - Reduced decay rate,
  - smaller size,
  - non-magnetic structure allowing for MRI PET gantries,
  - and equivalent gain and noise compared to PMT.
- High Z mirrored input for multi-path delivery
- High Pass filtered input with adjustable minimum Energy threshold



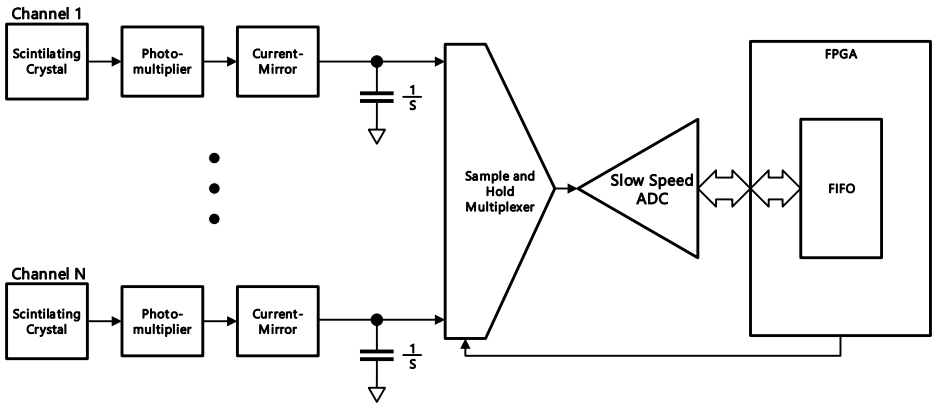
Measurement

Post-sample Digital Integration



- Advantages
  - Stable over temperature
- Disadvantages
  - Costly implementation
  - Requires high-speed ADC
  - One ADC per channel needed
  - Higher FPGA pin and fabric requirement

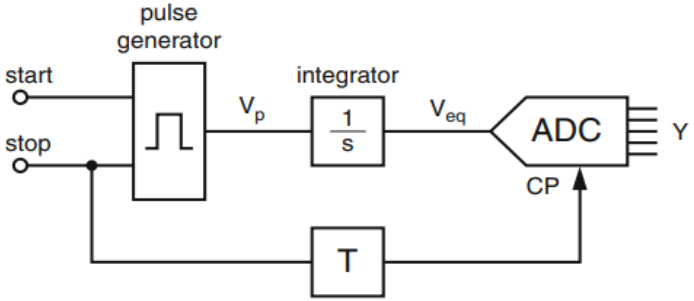
Pre-sample Analog Integration

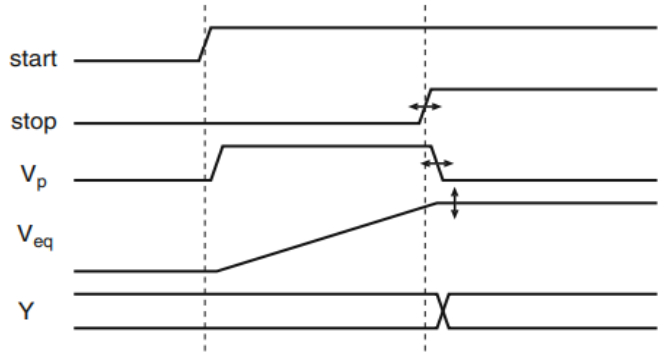


- Advantages
  - Cheaper implementation
  - Slow-speed ADC
  - One ADC per 8 or 16 channels
  - Lower FPGA pin and fabric requirement
- Disadvantages
  - Not as stable over temperature
- Chosen for implementation

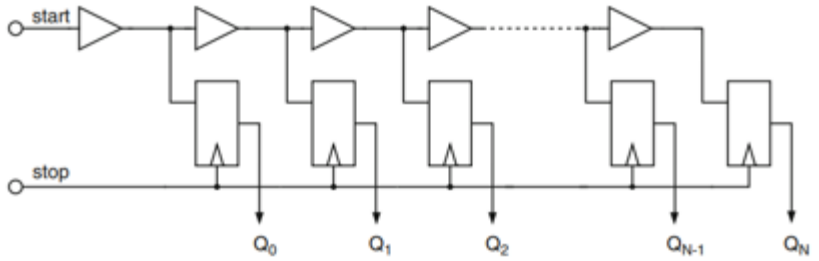
TDC TOF & TOT Measurement

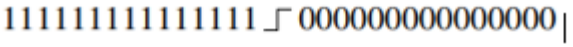
- Time-to-Digital Converter (TDC) Methods



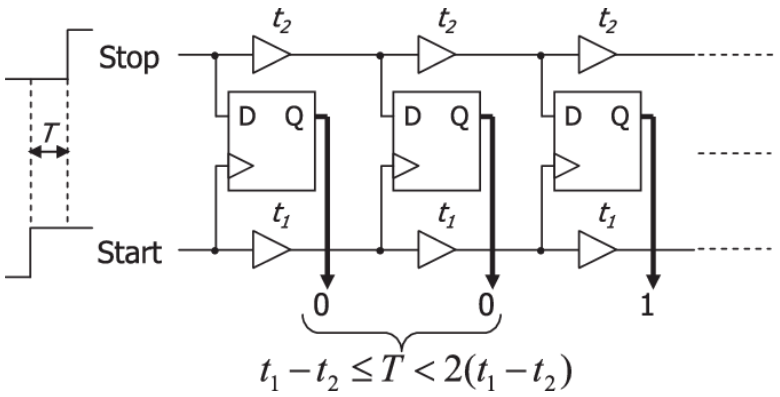


Analog





Digital "Pure" TDL



Digital Vernier TDL

TDC Previous Works

12 FPGA-based reference designs

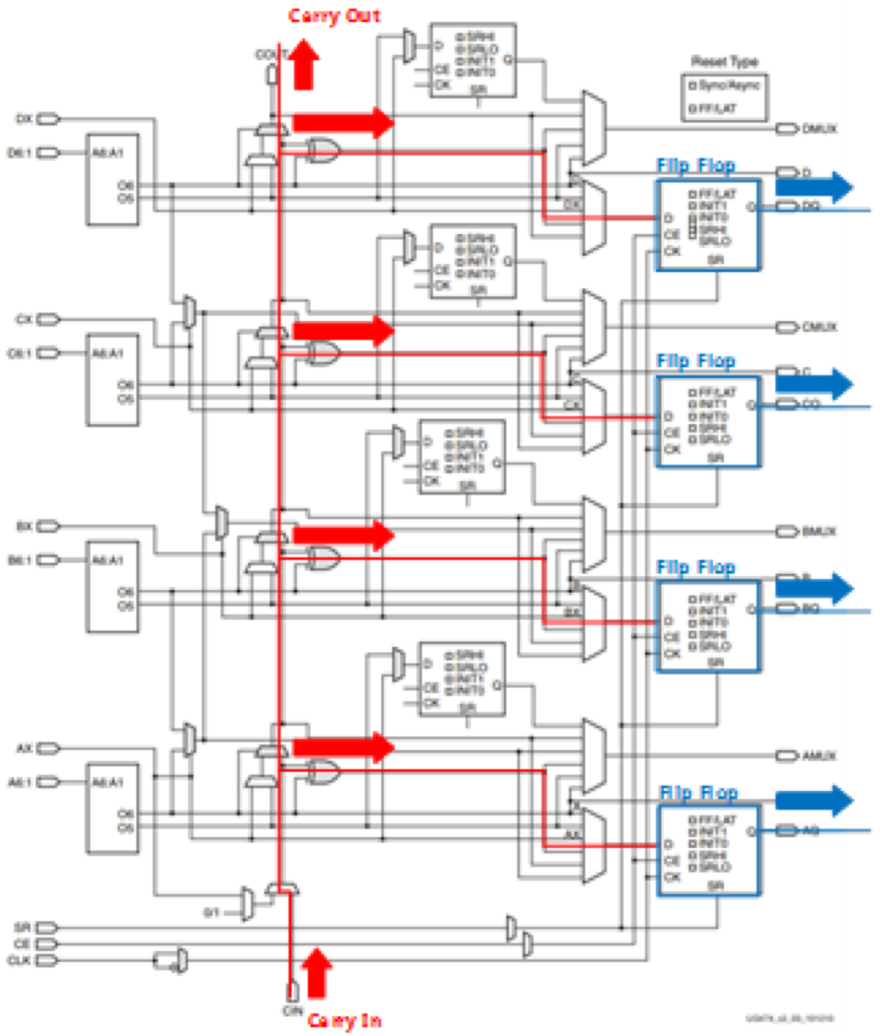
Ref.	Method	Year	RMS Resolution	Tech.	Integral Non-Linearity (INL)	Diff. Non-Linearity (DNL)
[19]	Vernier TDL	1997	200ps	650nm	<200ps	-94ps, +88ps
[20]	Vernier TDL	1997	129ps	650nm	46ps	-144ps, +214ps
[22]	Multi-phase clocks	2012	625ps	65nm	31.25ps	31.25ps
[23]	Pure Carry TDL	-	50ps	90nm	-	300ps
[15]	Pure Carry TDL	2009	17ps	65nm	-51ps, +43.86	-17ps, +60.35ps
[12]	Pure Carry TDL	2013	15ps	65nm	±60ps	-15ps, +45ps
[21]	Multichain averaging	2015	4.2ps	40nm	-28.7ps, +18.2ps	-2.9ps, +11.72ps
[24]	Matrix of counters	2017	7.4ps	65nm	11.6ps	5.5ps
[25]	Wave union	2008	10ps	90nm	-	-
[26]	Wave union	2013	7.7ps	65nm	-	-
[27]	Ring oscillators	2008	40ps	90nm	<40ps	<40ps
[28]	Ring oscillators	2017	50ps	350nm	±65ps	±35.75ps

All derived from "Pure Carry TDL"

TDC Delay Lines

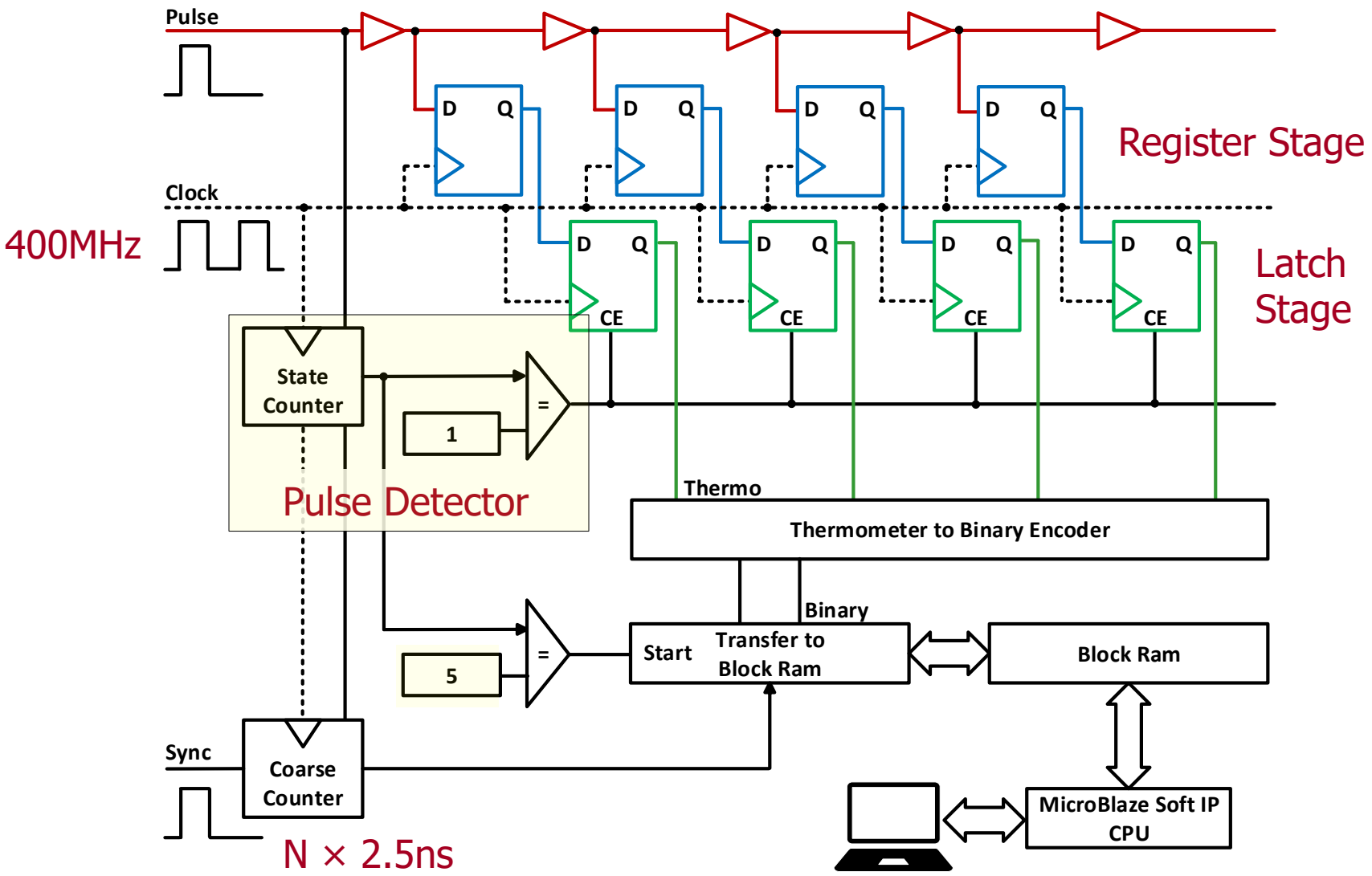
Pure Carry Tapped Delay Line

- Simplest implementation
- Lowest resources needed
- Better linearity vs. Vernier
- Core of most methods



Xilinx SLICEL with CARRY4 and first stage registers

TDC Initial Design



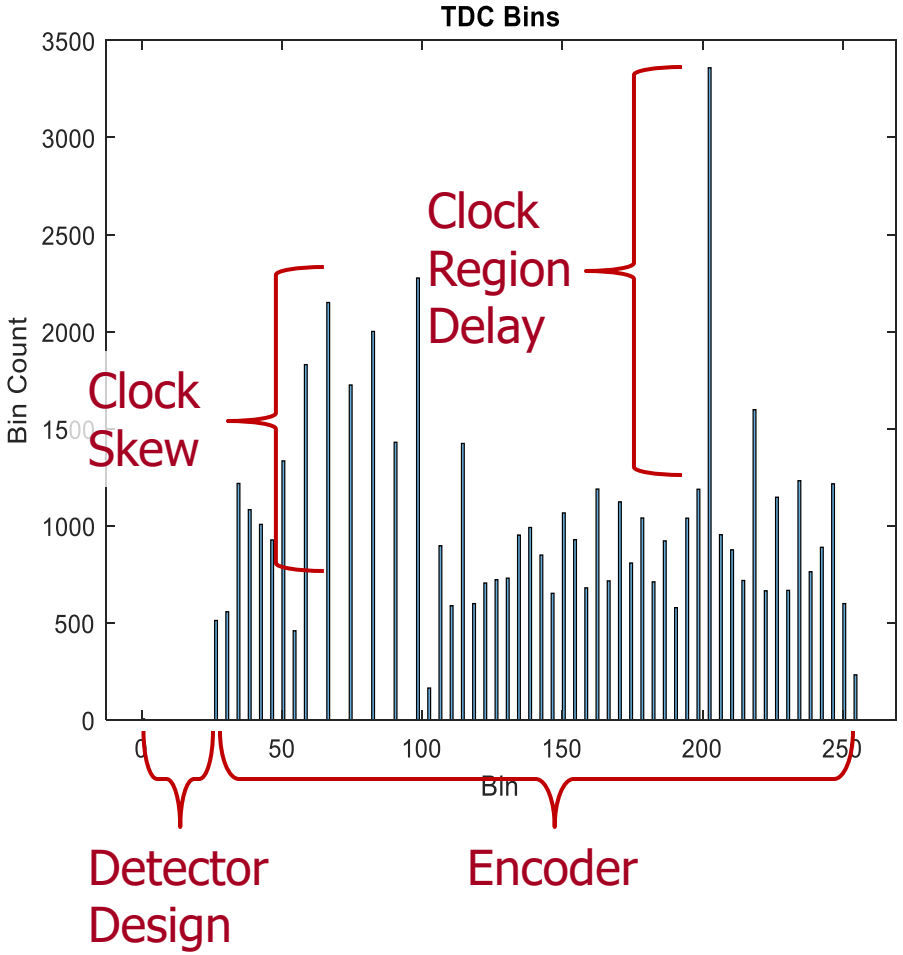
TDC Initial Results

Initial Design Issues

- Large quantity of zero length bins at front and throughout
- Very large bin at clock region crossing
- Significant nonlinearity

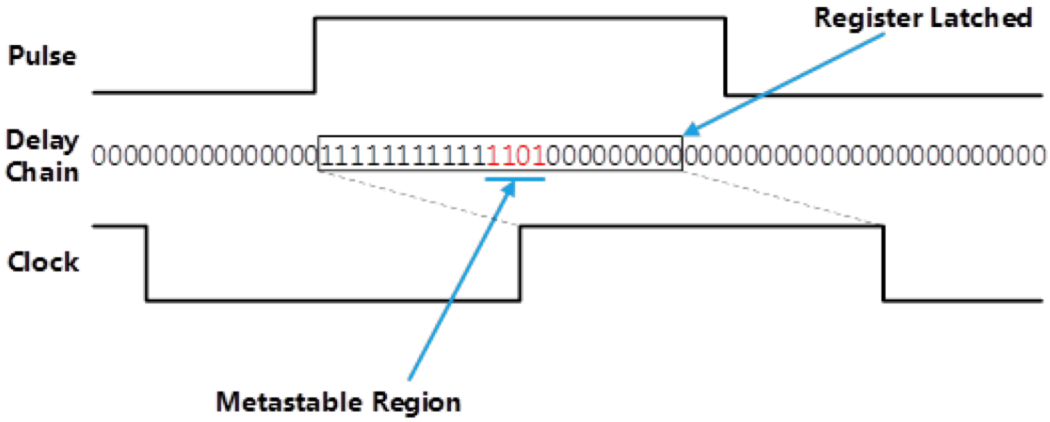
Causes

- Delay chain crosses fabric clock region boundary
- Detector latch enable delayed
- Encoder result latched too soon
- Clock skew



Bubble Error

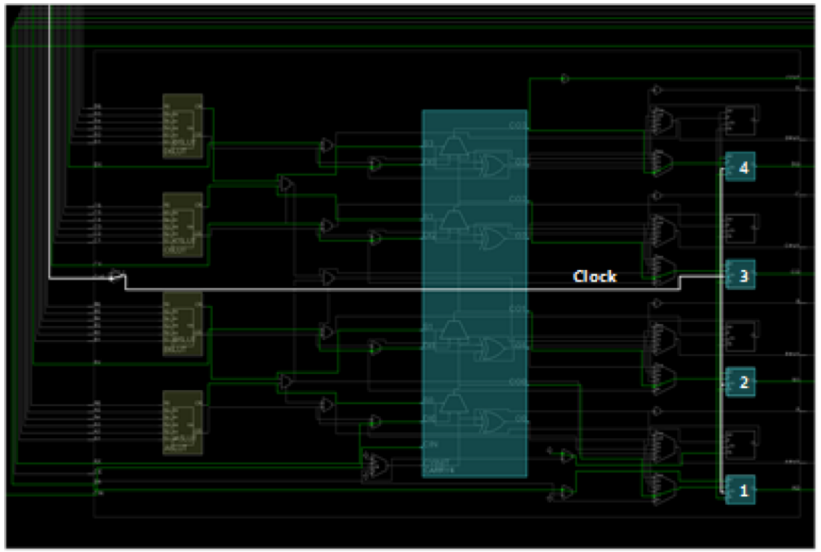
- The thermometer-to-binary encoder must handle bubble error.
- Review of the actual amount of unwanted '0's sandwiched between '1's revealed only one error
- "The Highest '1' (native)" encoder was chosen with modification for bin realignment



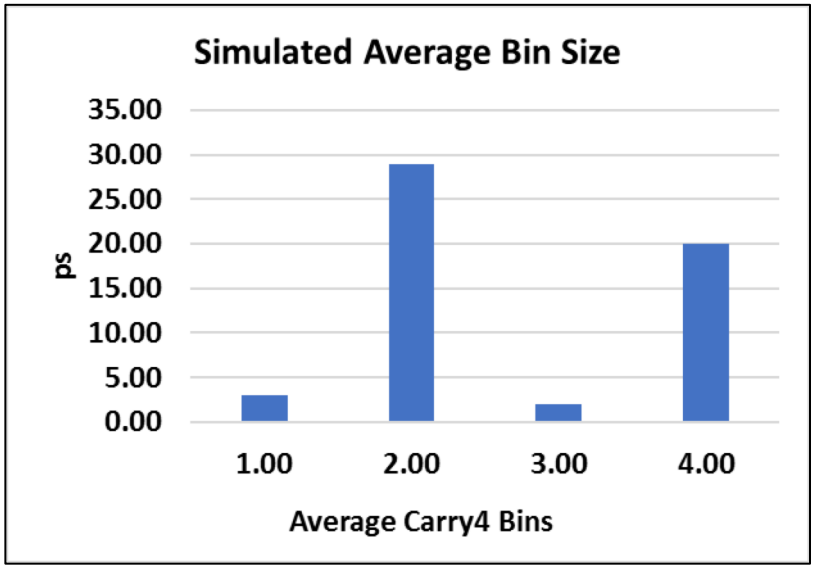

```
module thermo2bin #(parameter N = 50, bits = 8) (
    input reset,
    input clk,
    input [N*4-1:0] thermo,
    input rising_edge_In,
    output [bits-1:0] bin_Out
    );

reg [bits-1:0] bin, bin1;
integer i;

always @(thermo)
begin
    bin1 = 0;

    for (i=1; i<=N*4; i=i+1)
        begin
            if (thermo[i-1] == 1'b1 & thermo[i-2] == 1'b1) bin1 = i;
        else if (thermo[i-1] == 1'b1 & thermo[i-2] == 1'b0) bin1 = i - 1;
    end

end

assign bin_Out = bin1;

endmodule
```

Bubble Error Causes

- Clock skew causes later stage delay taps to be latched before the previous stage
- Notice how the clock is fed to registers 3, 2, and 4 before 1
- Simulation confirms this in predicted bin size

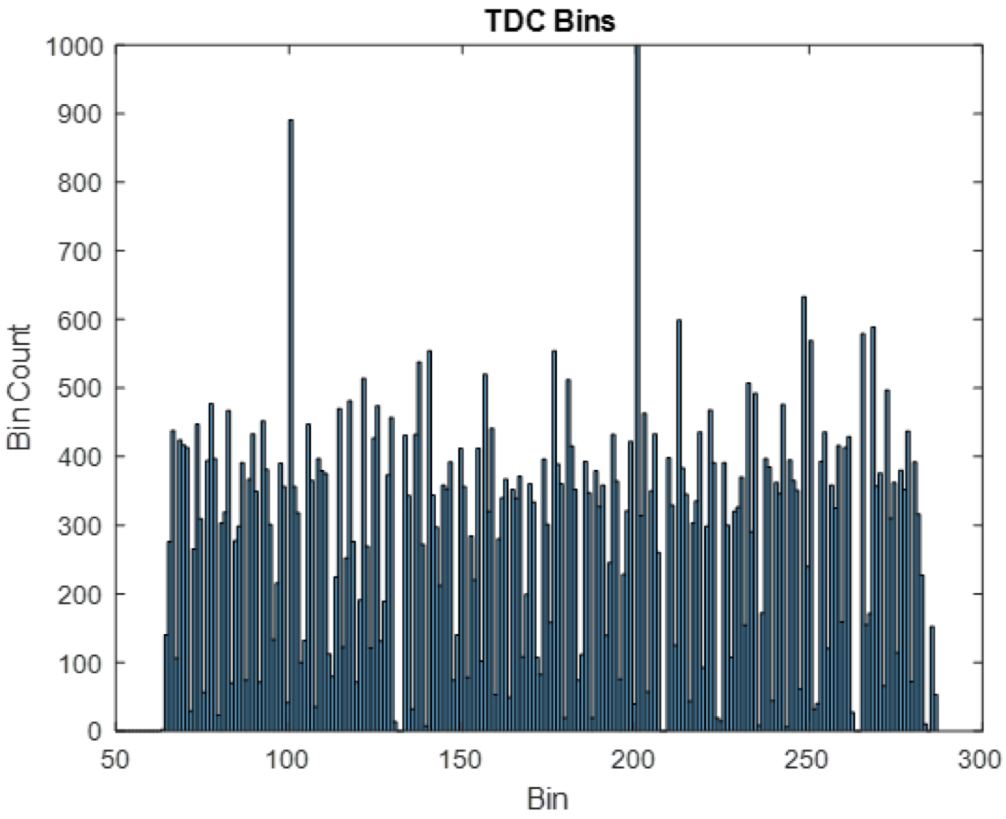


- Clock skew only becomes an issue with newer <40nm FPGAs
- Slower FPGA carry delays are >> than clock skew
- The KC705 eval board utilizes a 28nm -2 speed grade Kintex 7 with an average delay of 11ps



Bubble Error Solution

- Bin realignment helps to correct the effects of clock skew
- Analysis of Code Density testing and review of the thermometer code latched determines which bins must be realigned

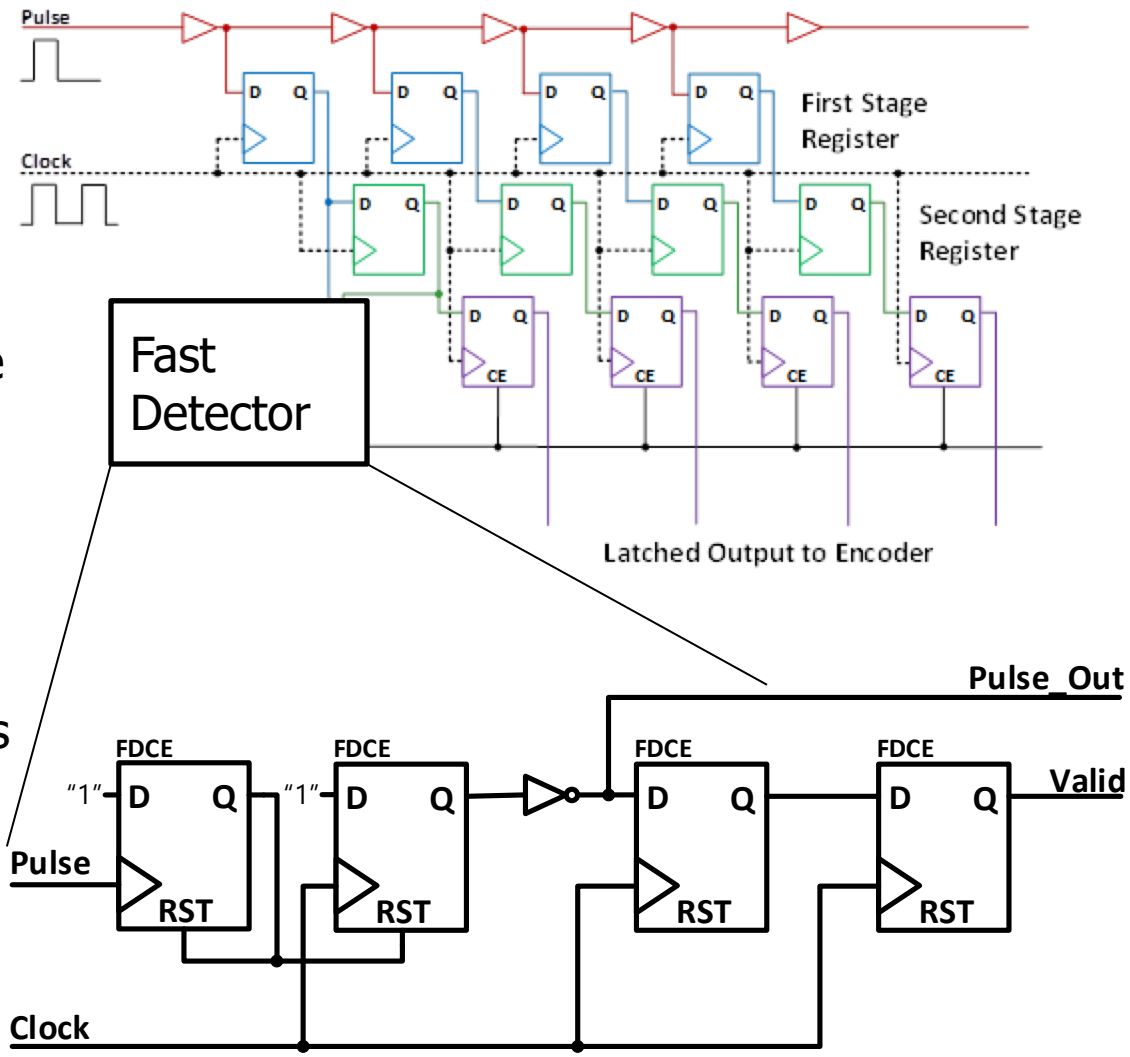


Results after bin realignment

TDC Pulse Detection

- Several iterations attempted
- Final selection feeds the pulse into the clock input of Flip-Flop and delays the pulse_out until the latch enable "Valid" signal has provided enough setup time for the latch stage

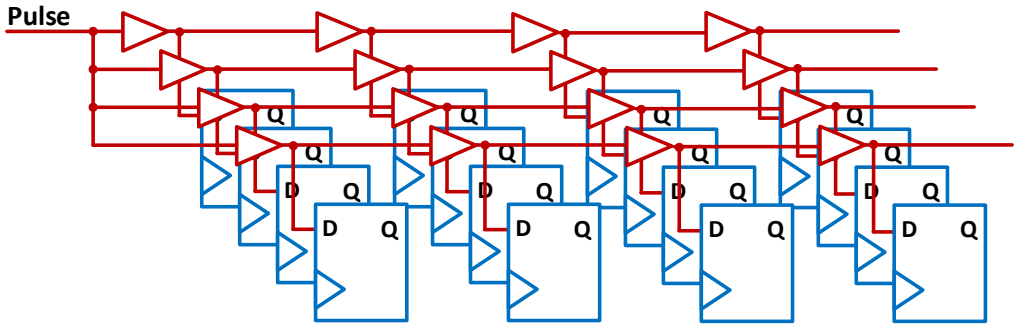
- This reduces the front bins from missing hits and allows for increased clock speed

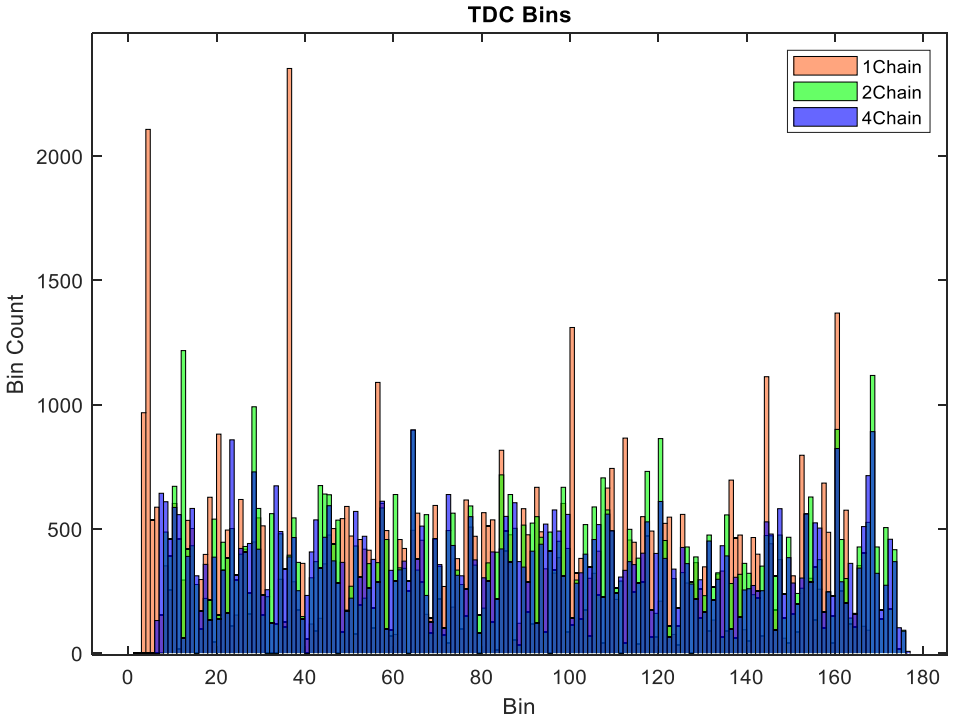


Final Detector Design

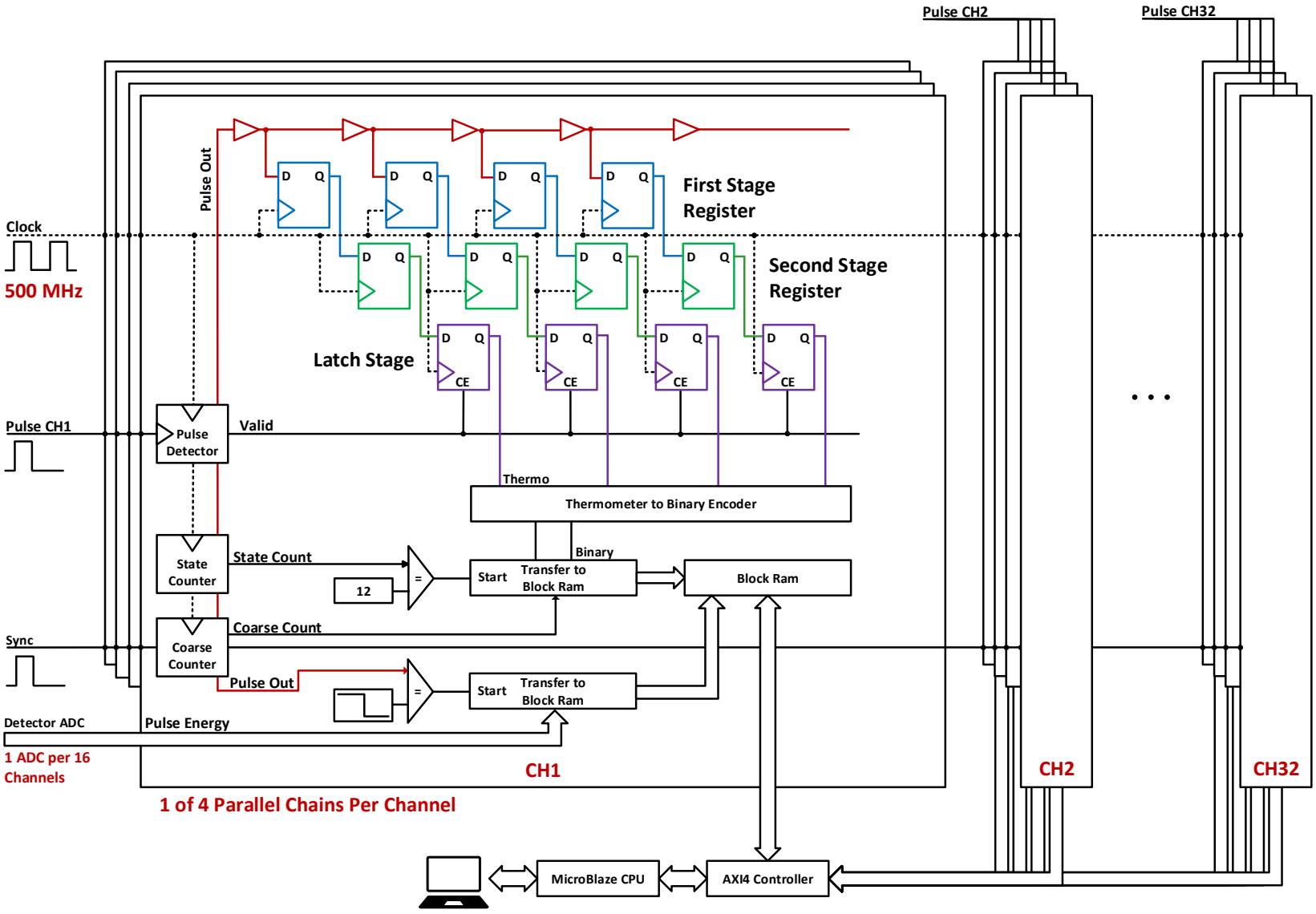
Multichain Averaging

- Multichain averaging is utilized for linearity improvement
- Results were ploted with 1, 2 and 4 parallel chains



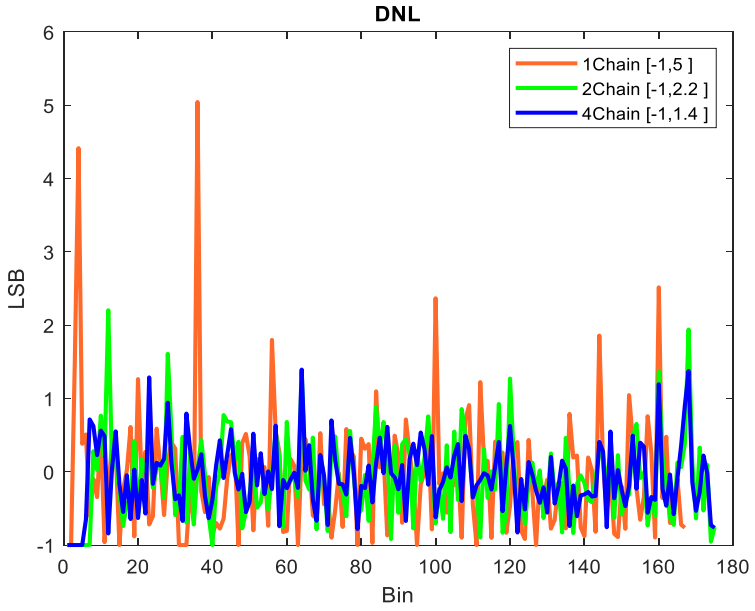


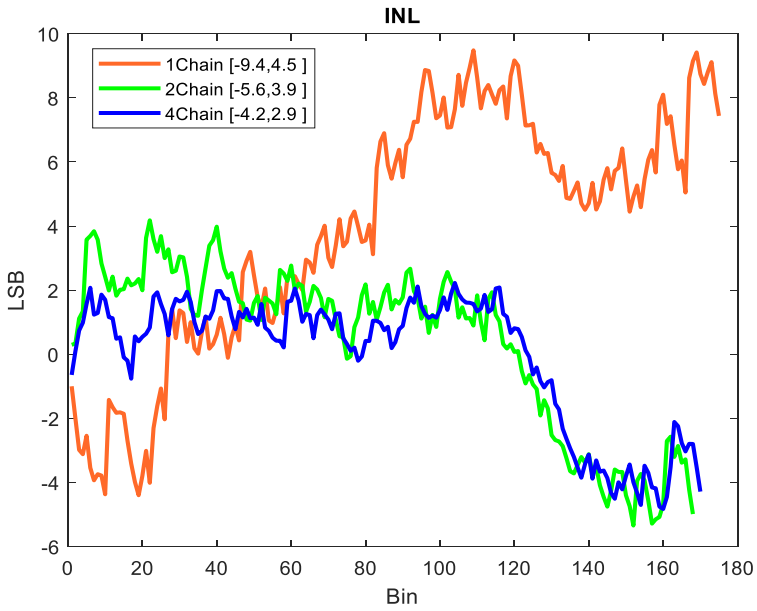
Final Design



TDC Linearity (Pre-Calibration)

Multichain Averaging

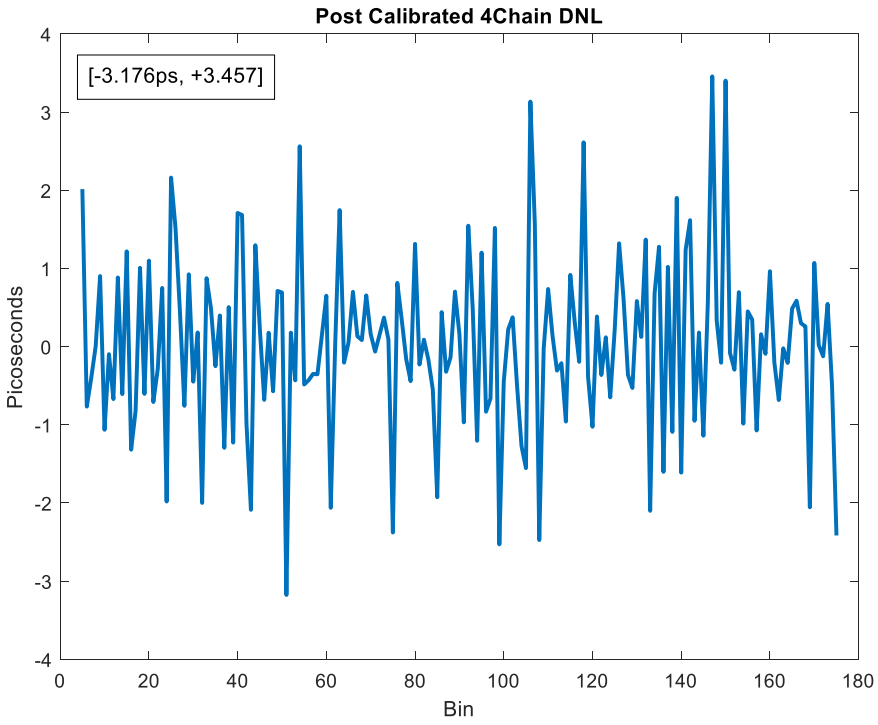


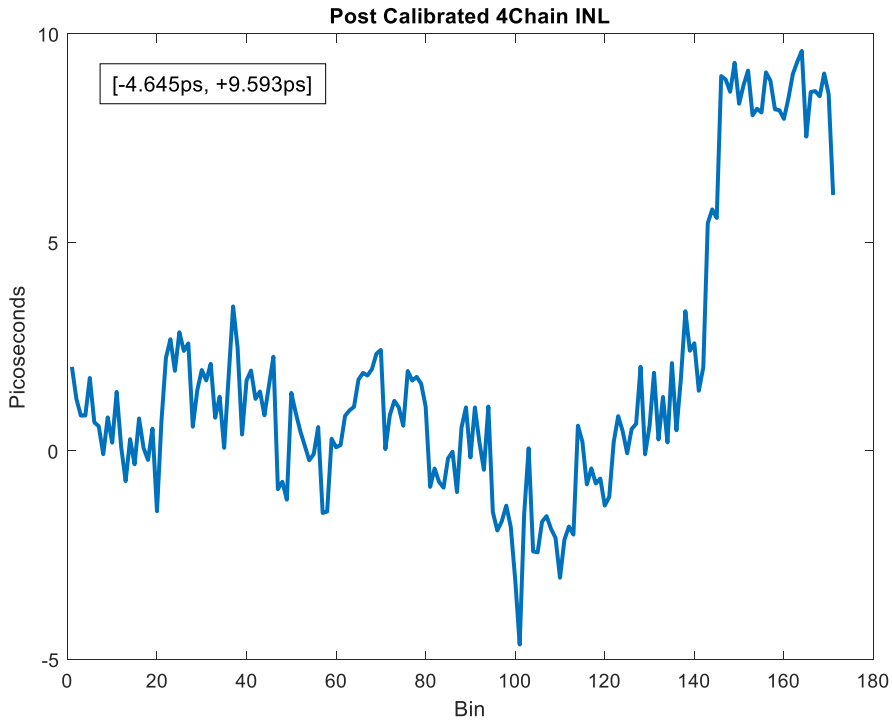


Method	DNL (LSB)	DNL (ps)	INL (LSB)	INL (ps)
1Chain	-1, +5	-11, +55	-9.4, +4.5	-103.4, +49.5
2Chain	-1, +2.2	-11, +22	-5.6, +3.9	-61.6, +42.9
4Chain	-1, +1.4	-11, +15.4	-4.2, +2.9	-46.2, +31.9

TDC Linearity (Post-Calibration)

4 Chain Averaging Results with Calibration

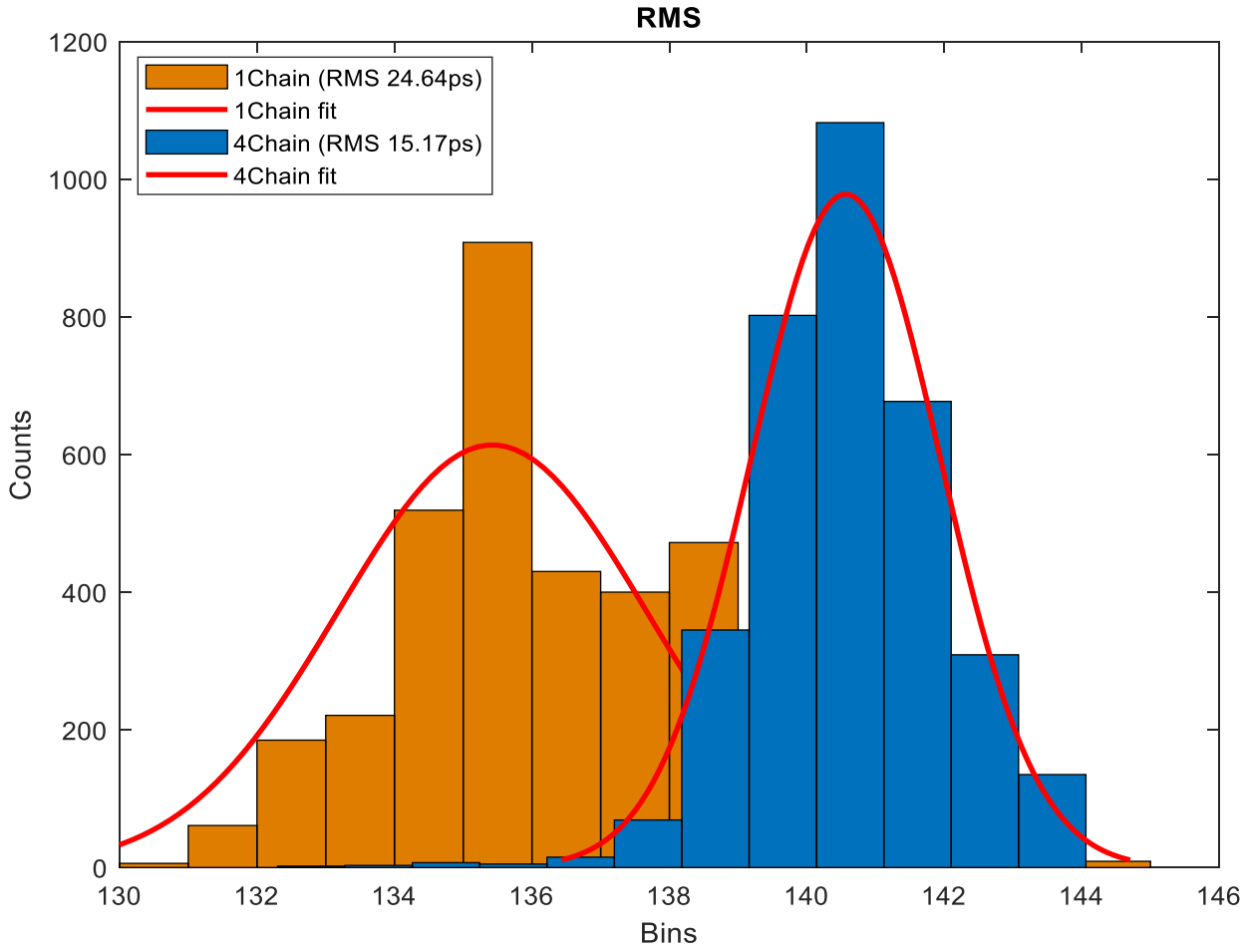




Method	DNL (LSB)	DNL (ps)	INL (LSB)	INL (ps)
4Chain	-0.29, +0.31	-3.18, +3.46	-0.42, +0.87	-4.65, +9.60

TDC Resolution

1 and 4 Chain RMS Results



TDC Results

Ref.	Method	Year	RMS Resolution	Tech.	Integral Non-Linearity (INL)	Diff. Non-Linearity (DNL)
	This Work (Multichain averaging)	2019	15ps	28nm	-4.65ps, +9.59ps	3.18ps, +3.46ps
[19]	Vernier TDL	1997	200ps	650nm	<200ps	-94ps, +88ps
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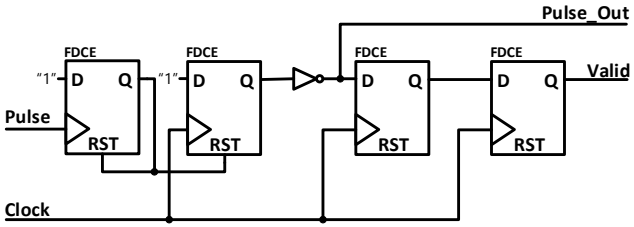
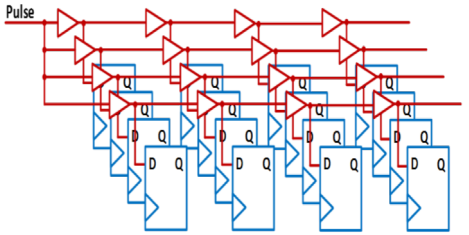
Best reported DNL and INL

Summary

- Analysis of challenges in FPGA TDC design
  - Nonlinearity, bubble error, bin realignment, pulse detection, clock region crossing, proper latching, metastability, calibration
- Contributed best-in-class multichain averaging TDC
  - 32 TDC Channel, 15ps, best linearity

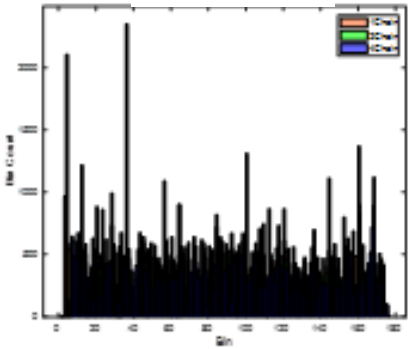


Fast Detector

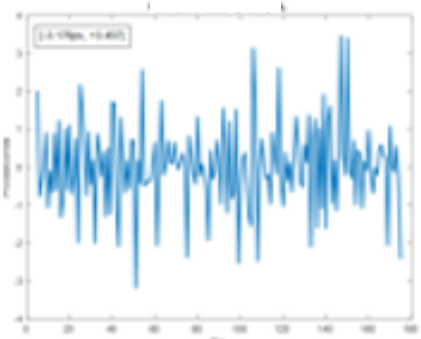


Multichain Averaging

4 Chain

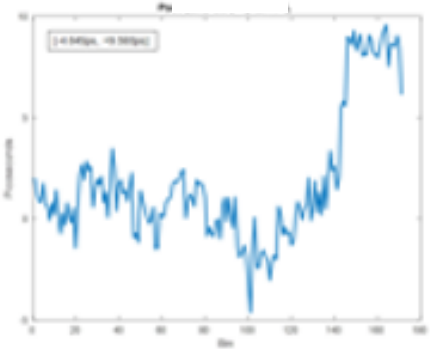


DNL



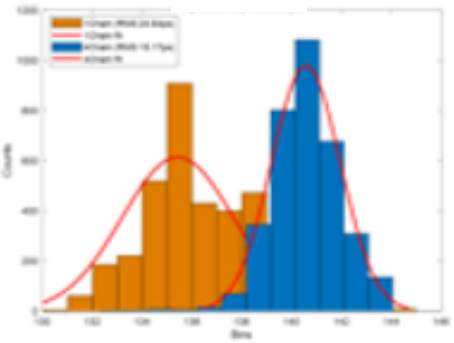
3.18ps, +3.46ps

INL



-4.65ps, +9.59ps

RMS



15ps

Thank you for your attention!

Q & A