Highly-linear FPGA-based Data Acquisition System for Multi-channel SiPM Readout

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Outline

- Motivation
- SiPM FPGA DAQ Architecture
- Detection
- Pulse Energy
- TDC
- Results
- Summary
Motivation

- Maximize input channels per FPGA for time-of-flight with energy measurement
- Utilize 28nm Kintex 7 FPGA for best price/performance/watt
- Simplify SiPM pulse energy measurement with interface to new UH designed detector
- Increased linearity
SiPM FPGA-based DAQ

Channel 1
- Crystal Scintillator
- Silicon Photomultiplier
- Current Mirror
- UH SiPM Detector
- HPF
- Comp
- DAC
- 1X
- ADC
- SiPM Detector Pulse
- Threshold Control
- 10 bit ADC Output
- SAR ADC CLK

FPGA
- TDC
- Energy Registers
- PLL & Derivative Clocks
- Processing Core
- DAQ Link
- TDC Clear (Sync)
- External CLK
- PC Link
- Up Stream
- Down Stream

Detection
Measurement
Event Processing

Channel 2
- *
- *
- *

Channel 32
Detection

- Selection of the scintillation material determines the gain and decay rate which dictates the full width half maximum TOF possible*
- Photomultipliers can be either a photomultiplying tube (PMT) or silicon based (SiPM)
- As resolution requirements increase, SiPMs are chosen due to their advantage with:
  - Reduced decay rate,
  - smaller size,
  - non-magnetic structure allowing for MRI PET gantries,
  - and equivalent gain and noise compared to PMT.
- High Z mirrored input for multi-path delivery
- High Pass filtered input with adjustable minimum Energy threshold
Measurement

Post-sample Digital Integration

• Advantages
  – Stable over temperature
• Disadvantages
  – Costly implementation
  – Requires high-speed ADC
  – One ADC per channel needed
  – Higher FPGA pin and fabric requirement

Pre-sample Analog Integration

• Advantages
  – Cheaper implementation
  – Slow-speed ADC
  – One ADC per 8 or 16 channels
  – Lower FPGA pin and fabric requirement
• Disadvantages
  – Not as stable over temperature
• Chosen for implementation
TDC TOF & TOT Measurement

- Time-to-Digital Converter (TDC) Methods

**Analog**

- Pulse generator
- Integrator
- ADC
- Output

**Digital “Pure” TDL**

- Start
- Stop
- Q0, Q1, Q2, ..., QN

**Digital Vernier TDL**

- Start
- Stop
- Delay time: $t_1 - t_2 \leq T < 2(t_1 - t_2)$
# TDC Previous Works

12 FPGA-based reference designs

<table>
<thead>
<tr>
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All derived from “Pure Carry TDL”
TDC Delay Lines

Pure Carry Tapped Delay Line
- Simplest implementation
- Lowest resources needed
- Better linearity vs. Vernier
- Core of most methods

Xilinx SLICEL with CARRY4 and first stage registers
TDC Initial Design

```
1. Transfer to Block Ram
2. Thermometer to Binary Encoder

Pulse Detector

State Counter

N x 2.5ns

Clock

400MHz

Register Stage

Latch Stage

CPU

MicroBlaze Soft IP
```

- **State Counter**: Initial state of the TDC
- **Pulse Detector**: Converts input pulses into digital signals
- **Register Stage**: Processes the data from the Pulse Detector
- **Latch Stage**: Captures and holds the processed data
- **Thermometer to Binary Encoder**: Converts the processed data into binary format
- **Start Transfer to Block Ram**: Initiates the transfer of data to Block Ram
- **Block Ram**: Stores the binary data
- **MicroBlaze Soft IP CPU**: Handles the processing and control of the TDC

The diagram illustrates the flow of data from input pulses to the final binary output, highlighting the key components and stages involved in the TDC design.
TDC Initial Results

Initial Design Issues

- Large quantity of zero length bins at front and throughout
- Very large bin at clock region crossing
- Significant nonlinearity

Causes

- Delay chain crosses fabric clock region boundary
- Detector latch enable delayed
- Encoder result latched too soon
- Clock skew
Bubble Error

- The thermometer-to-binary encoder must handle bubble error.
- Review of the actual amount of unwanted ‘0’s sandwiched between ‘1’s revealed only one error.
- “The Highest ‘1’ (native)” encoder was chosen with modification for bin realignment.
Bubble Error Causes

- Clock skew causes later stage delay taps to be latched before the previous stage
- Notice how the clock is fed to registers 3, 2, and 4 before 1
- Simulation confirms this in predicted bin size

- Clock skew only becomes an issue with newer <40nm FPGAs
- Slower FPGA carry delays are >> than clock skew
- The KC705 eval board utilizes a 28nm -2 speed grade Kintex 7 with an average delay of 11ps
Bubble Error Solution

- Bin realignment helps to correct the effects of clock skew
- Analysis of Code Density testing and review of the thermometer code latched determines which bins must be realigned

Results after bin realignment
TDC Pulse Detection

• Several iterations attempted

• Final selection feeds the pulse into the clock input of Flip-Flop and delays the pulse_out until the latch enable “Valid” signal has provided enough setup time for the latch stage

• This reduces the front bins from missing hits and allows for increased clock speed
Multichain Averaging

- Multichain averaging is utilized for linearity improvement
- Results were plotted with 1, 2 and 4 parallel chains
Final Design

Pulse CH1
Clock
500 MHz
Pulse CH1

First Stage Register
Second Stage Register
Latch Stage

Thermometer to Binary Encoder
Block Ram

Pulse Out
State Count
Coarse Count
Pulse Energy

1 of 4 Parallel Chains Per Channel
1 ADC per 16 Channels

Detector ADC
Sync

MicroBlaze CPU
AXI4 Controller

Pulse CH2
Pulse CH32

17
# TDC Linearity (Pre-Calibration)

## Multichain Averaging

<table>
<thead>
<tr>
<th>Method</th>
<th>DNL (LSB)</th>
<th>DNL (ps)</th>
<th>INL (LSB)</th>
<th>INL (ps)</th>
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<tbody>
<tr>
<td>1Chain</td>
<td>-1, +5</td>
<td>-11, +55</td>
<td>-9.4, +4.5</td>
<td>-103.4, +49.5</td>
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<td>2Chain</td>
<td>-1, +2.2</td>
<td>-11, +22</td>
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<td>-61.6, +42.9</td>
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<td>4Chain</td>
<td>-1, +1.4</td>
<td>-11, +15.4</td>
<td>-4.2, +2.9</td>
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[Graphs showing DNL and INL for different chain configurations]
TDC Linearity (Post-Calibration)

4 Chain Averaging Results with Calibration

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<th>DNL (ps)</th>
<th>INL (LSB)</th>
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<tr>
<td>4Chain</td>
<td>-0.29, +0.31</td>
<td>-3.18, +3.46</td>
<td>-0.42, +0.87</td>
<td>-4.65, +9.60</td>
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TDC Resolution

1 and 4 Chain RMS Results

![Graph showing 1 and 4 Chain RMS Results](image-url)
## TDC Results

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<td><strong>This Work</strong> (Multichain averaging)</td>
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Best reported DNL and INL
Summary

• Analysis of challenges in FPGA TDC design
  – Nonlinearity, bubble error, bin realignment, pulse detection, clock region crossing, proper latching, metastability, calibration

• Contributed best-in-class multichain averaging TDC
  – 32 TDC Channel, 15ps, best linearity
Thank you for your attention!

Q & A