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Highly-linear FPGA-based Data Acquisition System for Multi-channel SiPM Readout

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A 32 channel, 15ps resolution, Kintex 7 FPGA-based TDC DAQ for time-of-flight and time-over-threshold measurement is demonstrated along with a comparison to previous works. Results include 11ps mean bin size, less than 4ps differential nonlinearity, and less than 10ps of integral nonlinearity. Linearity is improved by multichain averaging with comparison of 1, 2, and 4 chains pre and post-calibration. Implementation difficulties including bubble error, zero length bins, inter-clock region nonlinearity, calibration, chain overflow are discussed with focus on modern FPGA concerns including clock skew and bin realignment. Measurement methods are reviewed as well as a comparison of common TDC methods.

Summary

Use of high linearity, high resolution, multi-channel, data acquisition (DAQ) systems for readout of highly sensitive silicon photomultipliers (SiPMs) is required for many high-energy physics experiments. SiPMs offer distinct advantages compared to photomultiplier tubes (PMTs) including insensitivity to magnetic fields, very fast response, low bias voltage, and miniaturization. FPGA advancements continue to shorten the gap between application specific integrated circuits (ASICs) and FPGA-based TDC performance for use in DAQs. Although FPGAs are limited to predefined fabric structure and architecture, use of linearization improvement techniques including wave union and multi-chain averaging are more easily implemented due to an abundance of carry chains and digital signal processing blocks. Common implementation difficulties have plagued FPGA-based TDCs since the 1990s including bubble error within the thermometer-to-binary encoder, inter-clock region nonlinearity, and calibration. Modern FPGAs exhibit new challenges due to advancements in fabric speed which shorten the difference between gate delay and path delay causing clock skew. As the gate delay of a common carry chain is reduced, small differences in the arrival time of a global clock to each tapped delay register causes a disparity between bin sizes often resulting in zero length bins. The solution is bin realignment and careful selection of a bubble correcting thermometer-to-binary encoder. Within this paper, implementation of a 32 channel, 15ps TDC using a Xilinx Kintex 7 FPGA will be reviewed along with an examination of each difficulty.

First, the standard code density characterization method will be explained along with a description of common TDC methods including advantages and disadvantages. Next, a basic time-of-flight TDC design will be reviewed with an evaluation of the code density histogram outlining each nonlinearity. The cause of each nonlinearity will be addressed with a specific change to the original design including explanation and reasoning. The final design includes a pipeline enabled pulse detector reducing front-end zero bins, a double buffered latching stage for metastability improvement, a fast thermometer-to-binary encoder tailored to handle bin realignment and increase clock speed, and a set of four parallel chains used for multi-chain averaging with focus on linearity improvement. Calibration is accomplished by the code density method using an onboard asynchronous clock fed to each input and storing the known bin lengths into block ram for use on subsequent runs. Use of a multiplexing technique to increase energy measurement channel count is proposed along with a final detailed DAQ design including snapshots of the Xilinx Vivado block design with onboard Microblaze processor. The final design including 32 channels, 15ps of RMS resolution, 11ps mean bin size, less than 4s differential nonlinearity, and less than 10ps of integral nonlinearity is compared to 12 previous publications with this work's linearity superior to all previous designs.

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