Development of Readout Electronics for a Digital Tracking Calorimeter

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Bergen pCT Collaboration

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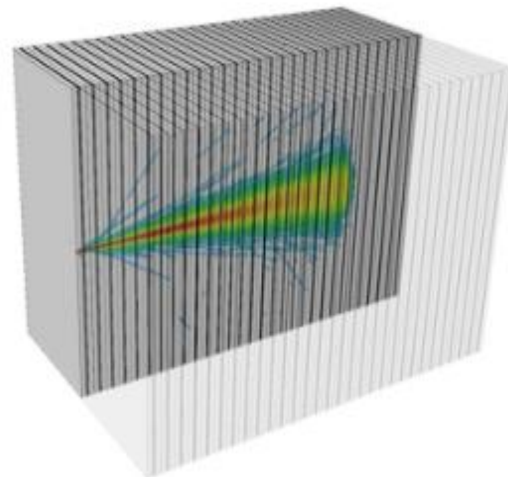
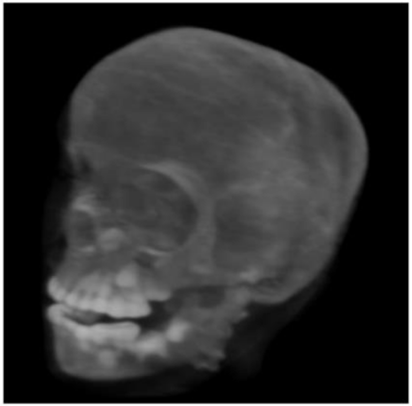
Digital Tracking Calorimeter

- Multiple layers of high-granularity pixel detectors
  - With absorption/conversion layers
- Tracking of individual particles
- Energy corresponds to path length
- Use cases:
  - A forward calorimeter at the ALICE experiment
  - medical imaging: proton CT (pCT)



Bergen pCT

- Goal: improve accuracy of particle radiotherapy
- 41 planes/layers of pixel detectors
  - Monolithic-Active Pixel Sensors
  - 27 x 18 cm
- Incoming beam parameters
  - Beam optics
- Post-phantom angle measurement:
  - Very thin front-tracker layers
- 3.5 mm thick Al absorber between layers
- 3D map of stopping power



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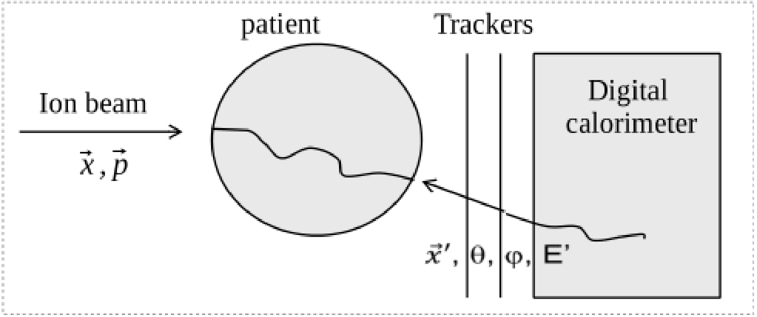
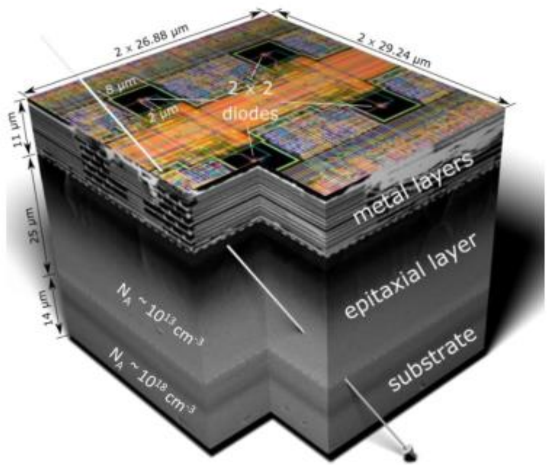


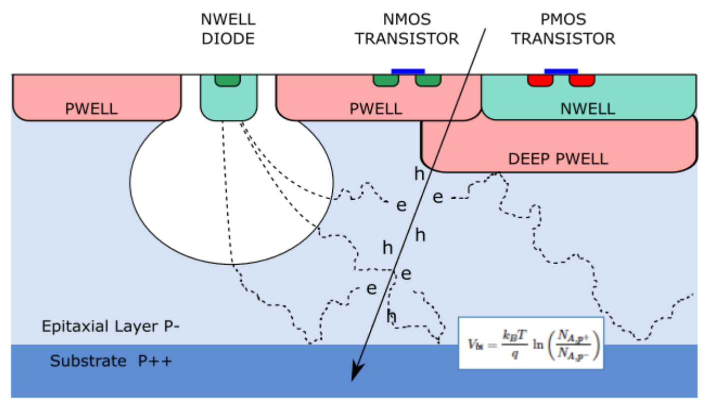
[1] V. A. Bashkirov, R. P. Johnson, H. F.-W. Sadrozinski, and R. W. Schulte, "Development of proton computed tomography detectors for applications in hadron therapy," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 809, pp. 120–129, 2016.

ALPIDE – ALICE Pixel Detector

- Pixel detector developed for ALICE ITS
- Monolithic Active Pixel Sensors (MAPS)
- Chip size: 1.5 cm x 3 cm
- Integration time: order of µs

- 1024 x 512 pixels
- Pixel size: 27 µm x 29 µm
- Digital readout: 1.2 Gb/s (8B10B)
- Each pCT Layer: 108 ALPIDEs



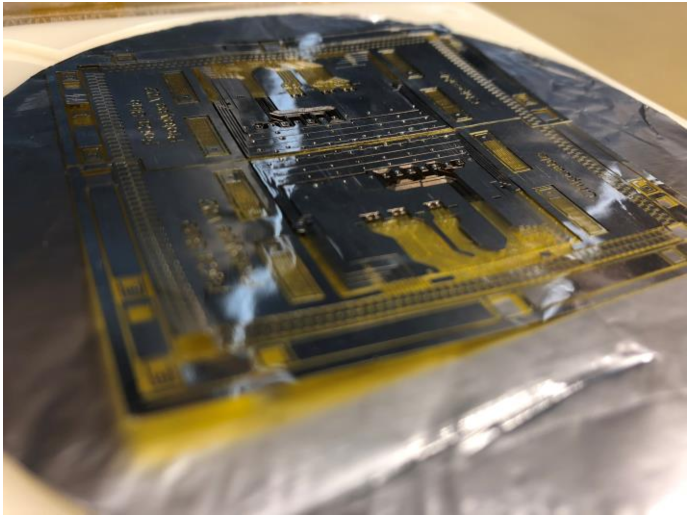


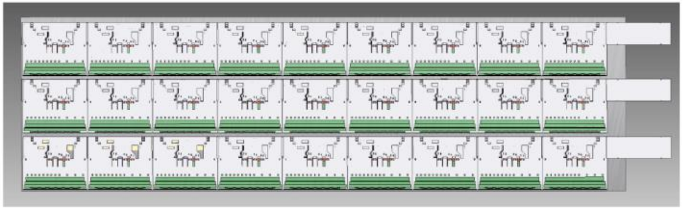
Design Challenges

- Structure requirements
  - Homogeneity
  - Density of connections
- High number of high-speed I/O-pins required
  - 108 x 1.2 Gb/s LVDS pairs
- High occupancy
  - Quasi-online dose planning tool
- Limited on-chip memory available
  - Possible back-pressure if not offloaded quickly

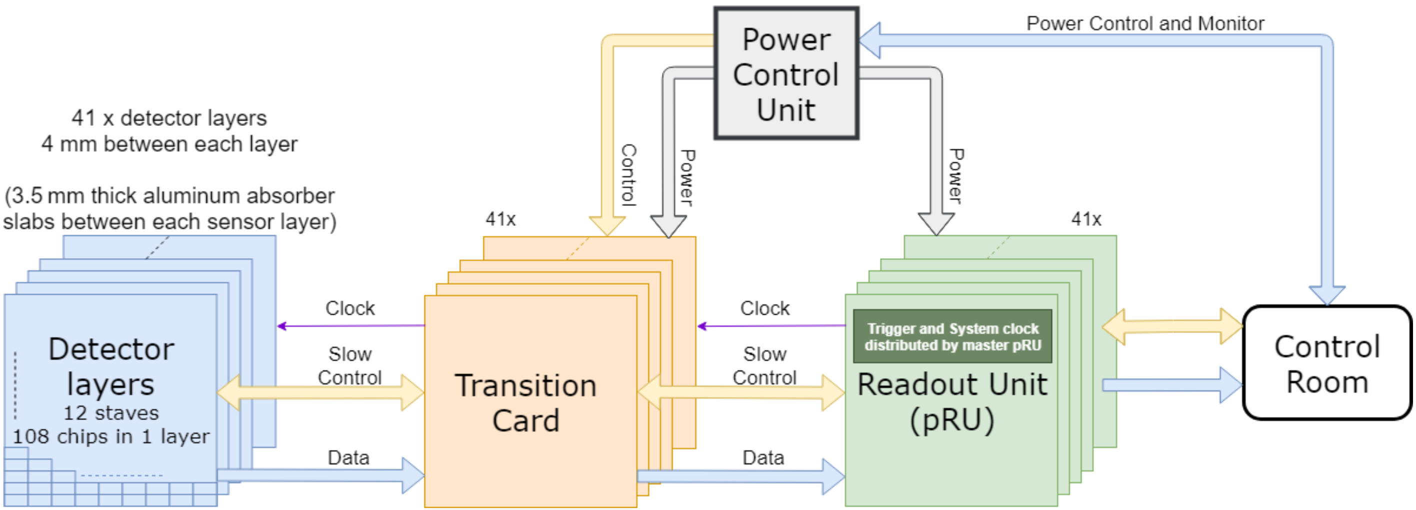
ALPIDE bonding and layer design

- ALPIDE mounted on thin cables
  - LTU, Kharkiv, Ukraine
  - Ultrasonic welding / Single-point Tape-Automated Bonding (SpTAB)
  - Aluminum-polyimide
    - (30 µm Al, 20 µm kapton)
- Carrier modules with 3 x 9 chips
- Layers with 4 carriers, i.e. 108 ALPIDEs

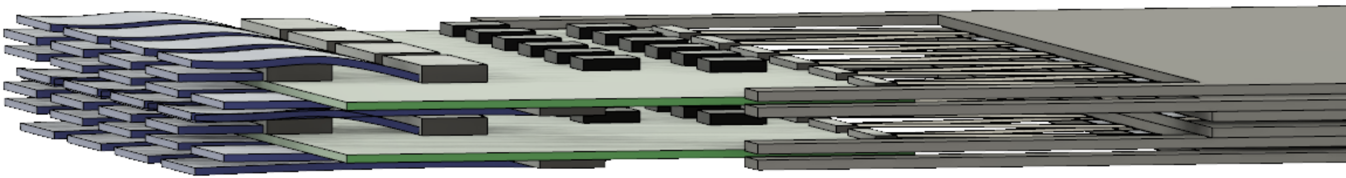


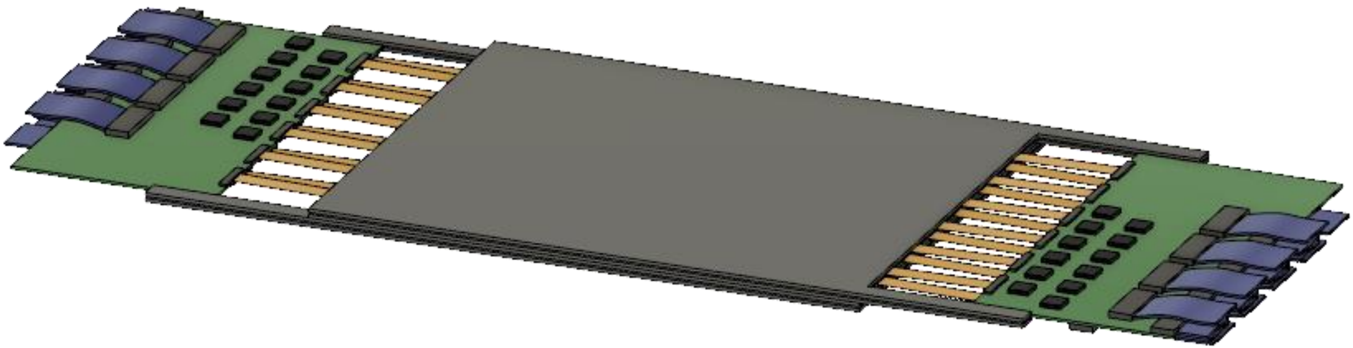


pCT Readout System Overview



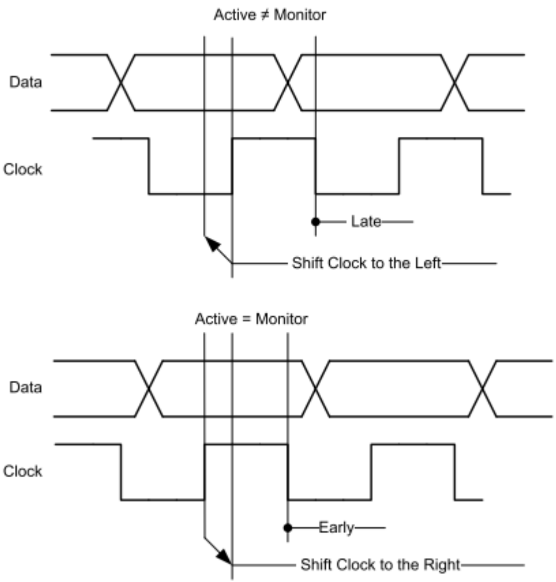
Physical and Electrical Design



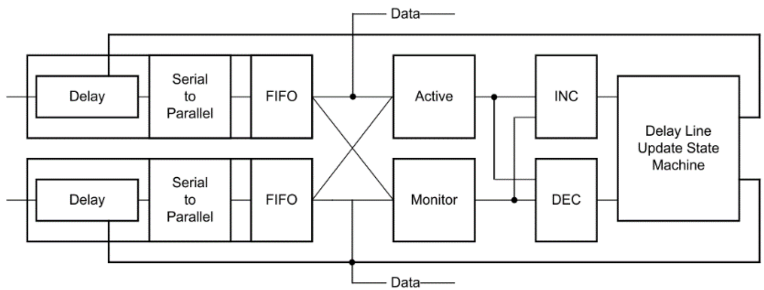


How to interface 108 1.2 Gb/s links per layer?

Alignment and Tracking Circuit (XAPP1274)



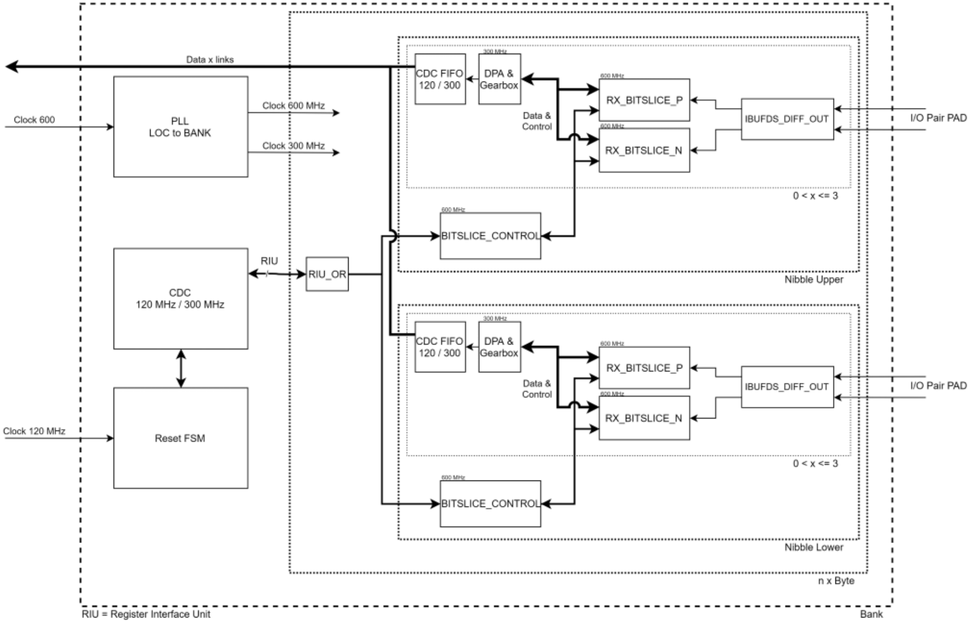
Xilinx XAPP1274

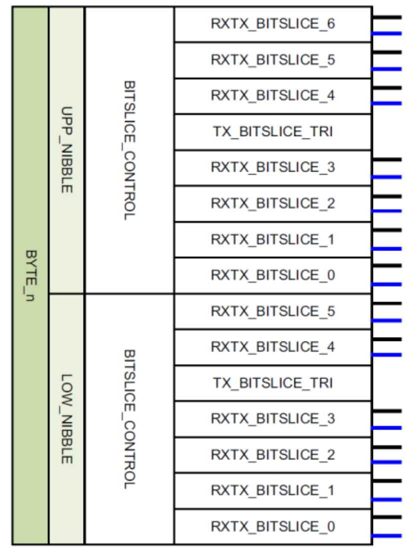


Xilinx XAPP1274

- Delay P&N ½ clock period
  - Steps in order of ps (512 steps per clock period)
- Continuously Monitor P&N variations
  - Alexander Bang-Bang Phase Detector
- Use delay to sample either P or N in the middle of eye
  - Update freq: 300 MHz
- Large variations or steps may cause bitslips

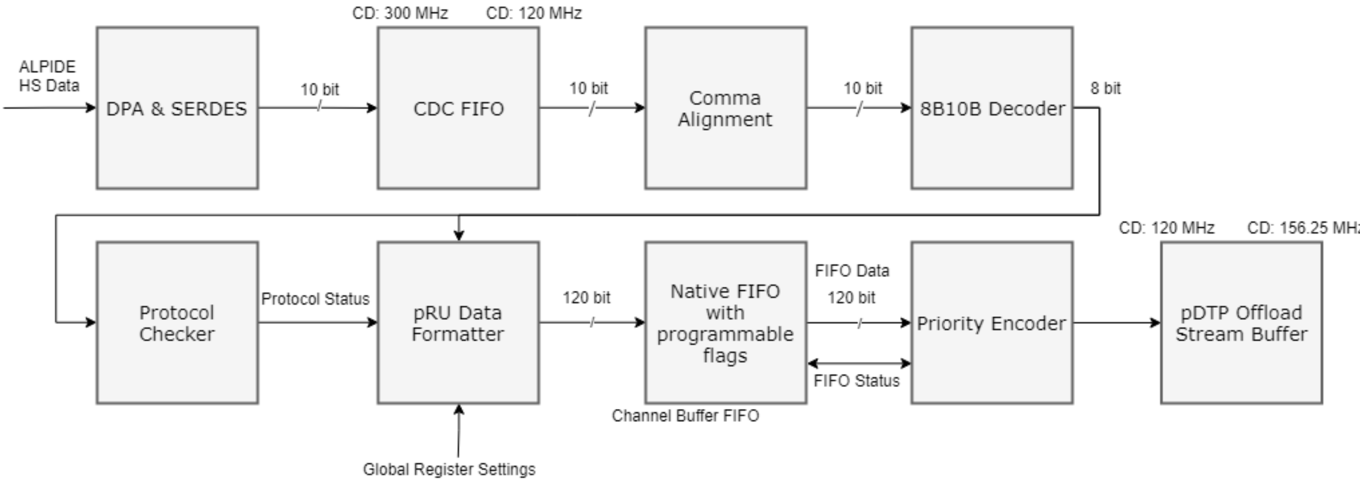
I/O Bank Firmware Design





Layout of Byte in I/O Bank
Xilinx XAPP1274

High-Speed Data Flow



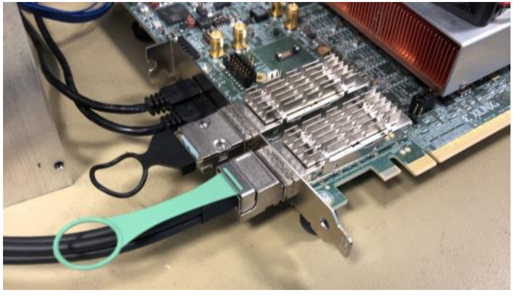
Results

- Bit Error Rate (BER) equivalent to Multigigabit Transceiver implementation
  - Measured Pseudorandom Binary Sequence BER $< \mathbf{9 \times 10^{-15}}$
- Equalization sweet spot requires manual sweeping
  - Separate bitstream
- Some errors are observed during data-taking
  - Dependent on activity on sensor, i.e. jitter
  - Also seen in Multi-Gigabit Transceivers (MGT) approach
- Conclusion:
  - Success!
  - Ultrascale FPGA: factor of 4 increase of possible links per FPGA

How to avoid back-pressure with minimal on-chip buffer?

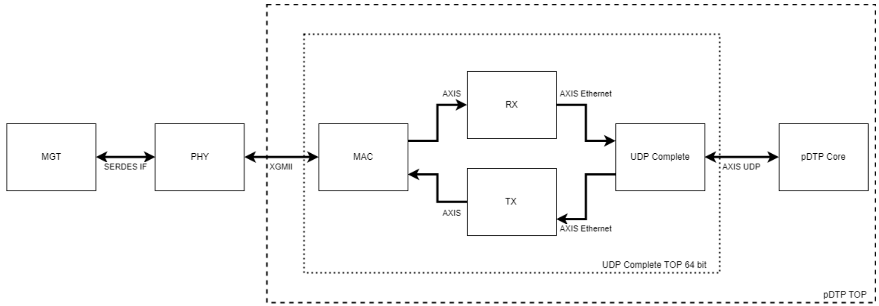
40 Gb/s UDP + custom protocol

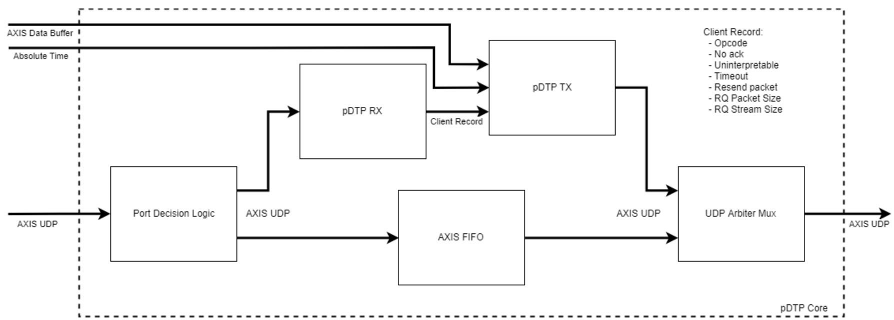
- QSFP+
  - Copper or optical
  - 4 x 10 Gb/s
  - Test setup: 1 x QSFP+ split to 4 x SFP+
- Complete open-source UDP/IPv4/Ethernet hardware stack for FPGA
  - See https://github.com/alexforencich/verilog-ethernet
- No need for embedded processors, DMA, …
- Custom data transfer protocol (pDTP)



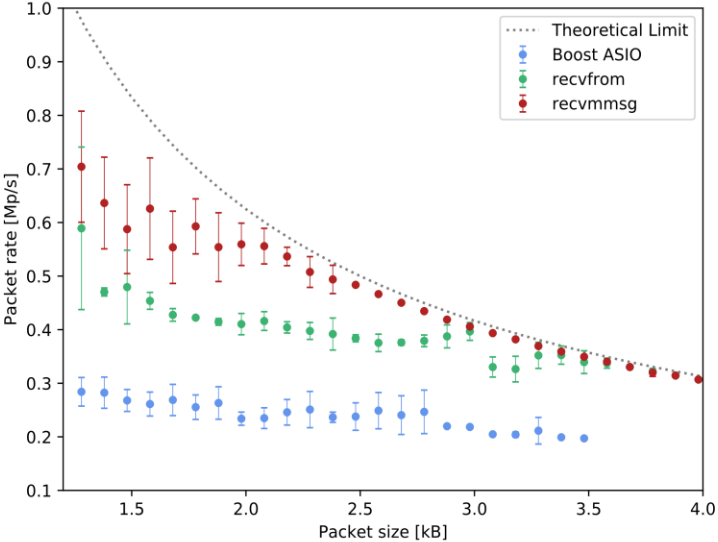
pCT Data Transfer Protocol (pDTP)

- Interface: AXI Stream
  - Connects to AXI Stream FIFO
- 3 modes:
  - Pull
  - Semi-push
  - Full-push
- Resending lost/dropped packets
- Throttling
- Extremely simple and lightweight
  - But powerful!





Results



- All modes: Good performance
- Push modes:
  - Close to theoretical limit
  - Limited only by host computer
- High latency
  - Round trip delay time up to ~30 µs
  - Only matters for pull mode
- Packet loss observed with small packets
  - Due to loss in RX buffer at host
  - Packet processing overhead
  - Solution: only transmit large packets

Summary

- SpTAB for homegeneous structure
- Regular I/O usage saves resources
- Hardware Implementation of UDP with custom protocol saves resources
- $\sim 4 \times 10^{12}$ pixels per second

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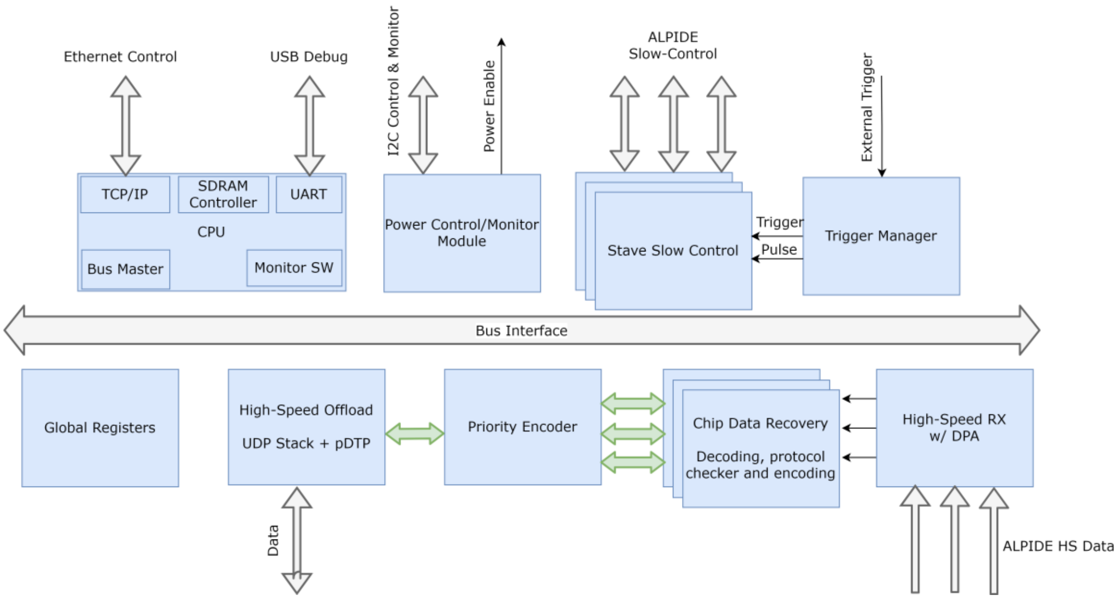
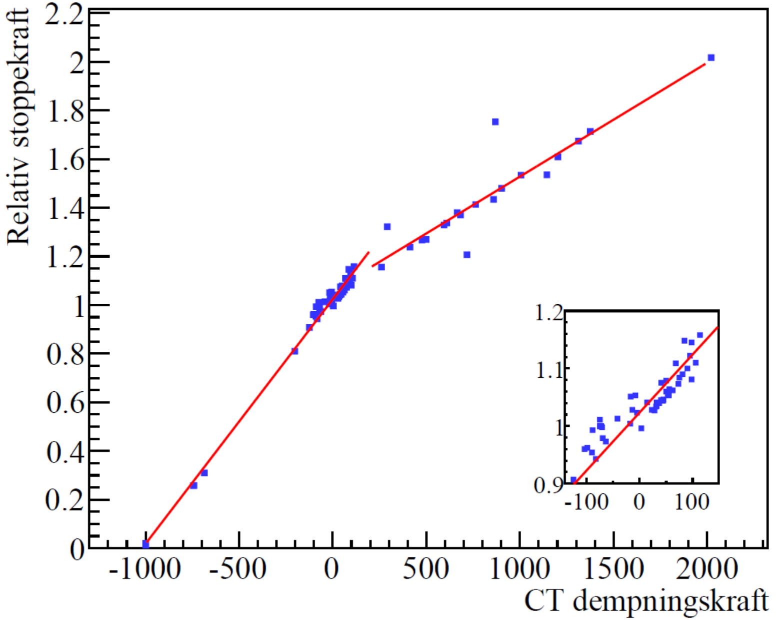
Backup Slides

Firmware Top-Level Design



CT Units to Relative Stopping Power



Pettersen, Helge Egil Seime, 'A Digital Tracking Calorimeter for Proton Computed Tomography' (University of Bergen, 2018)

Proton Therapy

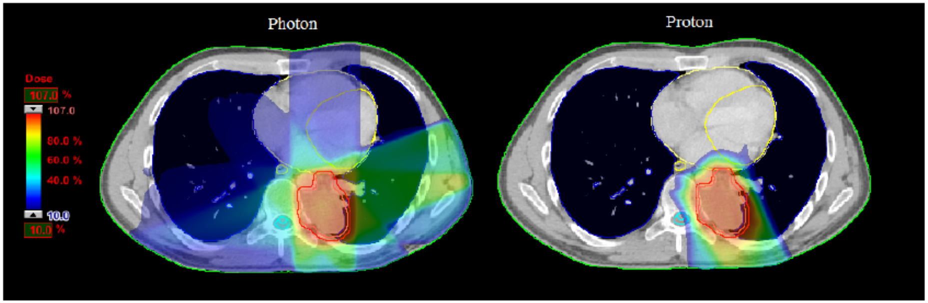


Figure 1.2: *A comparison between two dose plans for irradiation of a paravertebral sarcoma in the lung, overlaid on CT images.* ***Left:*** *(conventional) Intensity Modulated Radiation Therapy with photons.* ***Right:*** *Intensity Modulated Proton Therapy. Note the difference in volume between the low dose regions (the so-called low dose bath) visualized as blue areas, substantially smaller in the proton plan. Both plans are from G. M. Engeseth at Haukeland University Hospital, the plans are made using the Aria (version 11) dose planning system (Varian Medical Systems, CA, USA).*

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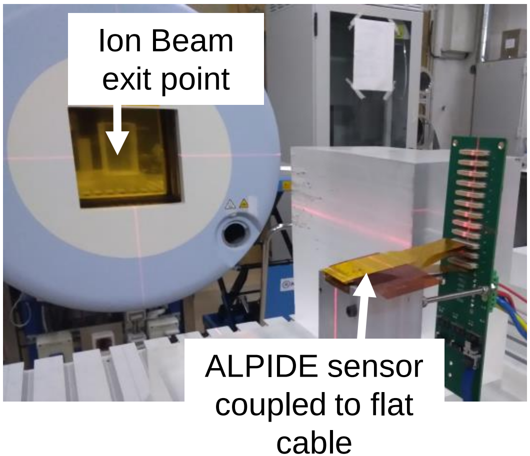
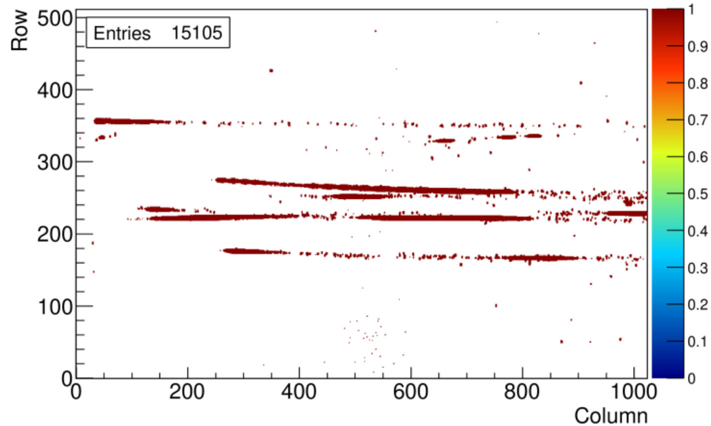
Heidelberg HIT Facility Experiment





Radiation Levels

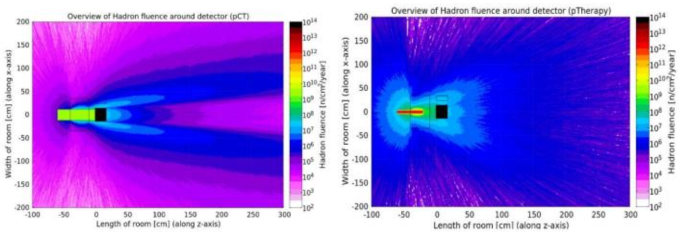


Figure 3: *The >20 MeV hadron fluence during the proton CT setting is shown in the plot to the left, and for proton therapy in the plot to the right. The results are normalized to be per year (#hadrons/cm²/year). The following geometries are marked: The water phantom (large rectangular outline), the first FPGA located at 10 cm (small rectangular outline) and the DTC (Black rectangle).*

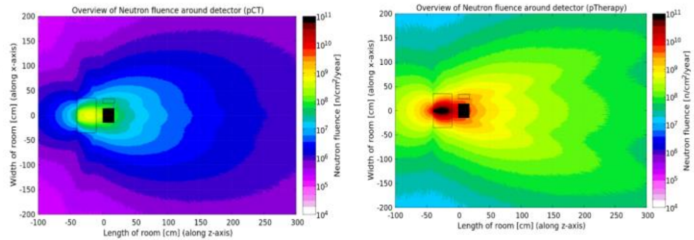
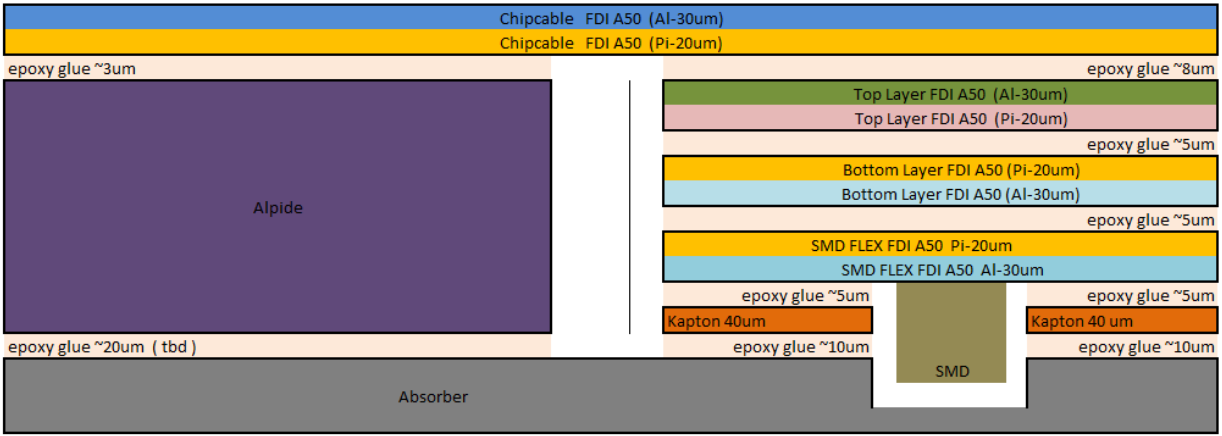


Figure 4: *The 1 MeV neutron equivalent fluence around the water phantom (large rectangular outline), first FPGA (small rectangular outline) and DTC (Black rectangle). The proton CT setting is in the plot to the left and the proton therapy in the plot to the right. Results are normalized to be per year (#neutrons/cm²/year).*

	Number of Single Event Upsets per year			
	FPGA10	FPGA50	FPGA100	FPGA200
Proton CT	26	2	0.3	0.06
pCT+pTherapy	1550	110	24	5

Conservatively, every ten bitflip will cause a functional error in the FPGA (Røed, 2017).

Cross-section



ALPIDE Pixel Circuitry