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Development of Readout Electronics for a Digital Tracking Calorimeter

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Highly segmented digital tracking calorimeters (DTC) consist of multiple layers of high-granularity pixel detector CMOS sensors and absorption/conversion layers. Two separate prototypes are being developed: (1) an electromagnetic calorimeter (FoCal) for a proposed ALICE upgrade (during LS3) and (2) a hadronic calorimeter for medical proton CT imaging (pCT). These prototypes employ the ALPIDE detector chip developed for the ALICE ITS. The ALPIDEs are mounted on intermediate Aluminum/Polyimide-flexible PCB with ultrasonic welding. This contribution presents findings and solutions to the challenging design of high-speed readout electronics with efficient use of FPGA resources for these prototypes.

Summary

Highly segmented digital tracking calorimeters (DTC) consist of multiple layers of high-granularity pixel detector CMOS sensors and absorption/conversion layers. Two separate prototypes are being developed: (1) an electromagnetic calorimeter (FoCal) for a proposed ALICE upgrade (during LS3) and (2) a hadronic calorimeter for medical proton CT imaging (pCT).

The pCT implementation of a DTC consists of 41 layers of 108 ALPIDEs each (˜ 27 × 18cm), where 9 chips are mounted together on a stave. The chips are mounted onto thin flexible Aluminum/Polyimide PCBs with ultrasonic welding. Three flex staves mounted on a thin Al-carrier form a basic module. Identical modules are the building blocks of the high-resolution layers of FoCal. Both prototypes have in common that they generate a large data rate locally due to high occupancy and that the designs are compact, i.e., the readout electronics has to handle a high density of high-speed links. In this contribution we are focusing on the pCT prototype.

The readout unit (RU) is interfacing all 108 x 1.2 Gb/s asynchronous data links in a layer, as well as all control and clock links. The RU consists of a Xilinx Ultrascale+ FPGA that is responsible for controlling the detectors and reliably transferring detector data upstream for processing.

The large density of high-speed links presents a challenge for the readout electronics. Few FPGA's have sufficient multi-gigabit transceivers (MGT) to interface the high number of asynchronous data links. However, newer generations of FPGA's have regular I/O-pins that are able to reliably sample up to 1.6 Gb/s data streams without the use of specialized transceiver pins. The downside of this is that no dynamic phase adjustment is presented to the user automatically and must be implemented manually in fabric logic. Employing Alexander (bang-bang) phase detection along with Xilinx I/O primitives to dynamically adjust the sample phase we achieve a link performance comparable to the MGT I/Os. This enables the use of fewer FPGA's per layer of the DTCs. On a Xilinx Ultrascale FPGA this increases the amount of possible links with at least a factor of 4 while also leaving transceiver pins available for other purposes.

The FPGA has a limited amount of on-chip memory. A high data burst size and rate from the sensors result in the need to offload the data from the RU in a highly efficient manner to avoid back-pressure and buffer overflow. Considering that all transceiver pins are still available, these can thus be employed for this purpose. Using QSFP+ we can implement 4 independent 10GBASE-R Ethernet channels transferring the data. A custom data transfer protocol, implemented in FPGA fabric for transmitting data via UDP without data loss, is under development. In addition, adopting Ethernet Jumbo frames will allow for a theoretical transfer efficiency of ˜

99% and thus, a total data rate of 39.6 Gb/s. This rate allows reading out up to a maximum ˜ 105 Gpixels/s per layer, and up to ˜ 4 Tpixels/s for the entire DTC.

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