Multi-channel time-tagging module for fast-timing Resistive Plate Chamber detectors

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- Proposed RPC for LHC upgrade
- TDC specifications
- Development of multi-channel TDC on FPGA Cyclone V
- Conclusion
Introduction

CMS muon upgrade at high eta

72 chambers to equip area with $1.8 < |\eta| < 2.4$

- Add track hits in muon reconstruction
- Search for Heavy Stable Charge Particle

Chamber dimensions:
165 cm x (63-114) cm

Need:
144 electronic readout board with 96-channel each
Introduction

Proposed double gap RPC

Double Gap layout

![Double Gap layout](image)

Y-position determination

\[ Y = f(t_{ext} - t_{int}) \]

On-detector Strip

Off-detector Strip

Principle of the readout electronics

Readout Board V0

Expected spatial resolution: 2 cm

Readout board
Introduction
Readout board prototype for system validation

Clock & control (CC) board

RPC

FE ASIC

FPGA (Cyclone V)

FEE board

TCP/IP link

PC:
Slow control & Acquisition

FEE board

Cyclone V

Requirement for FPGA-based TDC solution

- > 48 channels TDC / FPGA
- Full event-detecting efficiency
- Up to 16-channel simultaneous measurements
- < 20 ns dead time
- Better than 60 ps RMS (root mean square) time resolution
- Synchronization among several boards
Tapped-delay-line TDC

Typical architecture

- Measured signal
- Calibration signal

- Fast clock (e.g. 400 MHz)
- Slow clock (e.g. 100 MHz)

- Must be implemented in a small area for a good time resolution

- Encoder
- Counter
- Clock synchronization
- Look up table
- Pipeline

- Fine time
- Coarse time

Potential issue

Hundreds of logic state changes in a short time and a small space area

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TDC Implementation issue

VCC Sag and GND bounce (VSGB)

VCCIO (e.g. 1.15V)

VCC Sag ($\Delta V$)

$\Delta V = f(N, \Delta I, R_{wire})$

$\Delta T = f(N, \Delta I, R_{wire})$

Vin

Vout

R_{wire}

$\Delta V$

GND bounce ($\Delta V$)

<table>
<thead>
<tr>
<th>N</th>
<th>Number of gates and latches that switch in same time</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Delta I$</td>
<td>Relatively high $\Delta I$ for fast carry chain and high fan-out support DFF</td>
</tr>
<tr>
<td>R_{wire}</td>
<td>Relatively high value for Cyclone V (low power and low cost)</td>
</tr>
</tbody>
</table>

VSGB issue

1) Slow down edge of the input signal
2) Modify the input signal value (A,B) of adder

1) Degrade the accuracy of time-tagging measurements
2) Produce wrong signal detection

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Previous work: Implementation 2-Ch TDC

Normal signal input mode issue

E.g. input signal

<table>
<thead>
<tr>
<th>TDC clock cycle</th>
<th>N</th>
<th>N+ 1</th>
<th>N+2</th>
</tr>
</thead>
<tbody>
<tr>
<td>DFF output [500:0]</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VSGB => loop back noise propagate on the delay line

Proposed signal reshaping input mode

1) Shorten the signal transmission path
2) Change more quickly the input signal level of last ALM

Input signal

A(0) = '0'

B(0) = '1'

Sum(0)

1) DFF output [500:0]

<table>
<thead>
<tr>
<th>Cycle</th>
<th>DFF output [500:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td></td>
</tr>
<tr>
<td>&gt;N</td>
<td>&quot;....00000....&quot;</td>
</tr>
</tbody>
</table>

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Multi-channel TDC implementation issue

For the multi-channel TDC implementation

=> Increase average current

=> Simultaneous operations of several channels increase peak current

**Issue**

DFF bank example (using reshaping module for the input signal)

MSB

e.g. \[\ldots 11111101111\ldots11111011110\ldots101000000000100000\ldots\]

[0]

Signal edge

Transition area > 23 bit

Leading to serious nonlinear and wrong signal detection without special treatment
Proposed noise immune encoder

Noise filter based encoder

Signal’s leading edge validation

e.g.[63] [0]

Cycle : N-1 “....1111111111....”

Cycle : N “....100001010....”

Cycle : N+1 “....0000000000....”

Thermometer code pattern

converted One-hot code pattern

Output signal edge position
(1st metastable bit of transition area)

Found signal leading edge position

AND

Found signal leading edge

=> Noise immune

=> Full event-detecting efficiency
Proposed multi-channel TDC
Final Architecture

Measured signal
Calibration signal

Signal Reshaping

“0” “1” “0” “1” “0” “1” “0” “1”

DQ DQ DQ DQ DQ

Reduced pattern by 4 (160 bit)

Noise immune encoder

Counter

Clock synchronization

LUT

Fine time

Coarse time

Fast clock Domain: 400 MHz

Slow clock Domain: 100 MHz

MUX

“0”

DQ

(640 bit)

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Synchronization among different boards

TDC based solution

\[ T_{\text{final}} = T_{\text{measure}} - T_0 \] => synchronize several boards with precision of 1 LSB of TDC
Laboratory Test

Test setup with 56-CH TDC implementation on one FPGA

CC board

Reset

Sig

TDC[0]

T0

Tfinal

Tmeasure

Cyclone V

TCP/IP

PC
TDC calibration

Calibration channel by channel

DNL Range

INL Range

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RMS Spread (ps): 15 ps – 28 ps
RMS per channel ($/\sqrt{2}$): $\sim$11 ps to 20 ps

\[ \text{Tdiffent} = \sum_{k=0}^{55} \sum_{n=0}^{55} (TDC[n] - TDC[K]) \]

if $N \neq K$
Ongoing test on detector

Almost full efficiency

preliminary

COSMIC904: FEBv1.1b:iRETURN
1399: THR=88±10fC DT=10ns Filter LRpos

μ efficiency

cluster size, number of clusters, multiplicity

Cluster Size
Number of Cluster
HR multiplicity
LR multiplicity

AND: WP_1 = 7.38±0.06 (kV) EFF_1 = 0.970
HR: WP_2 = 7.36±0.06 (kV) EFF_2 = 0.978
LR: WP_3 = 7.36±0.06 (kV) EFF_3 = 0.972
Conclusion and perspectives

Conclusion

Successful implementation of multi-channel TDC on Cyclone V by using

- signal reshaping of the measured signal
- Noise immune encoder

The implemented TDC has

- Full event-detecting efficiency
- No-interference among channel

perspectives

- Development of radiation-tolerant TDC on FPGA

Thanks for your attention
Backup
TDC Implementation issue

E.g.

Signal

TDC Clock
(400 MHz)

T0 T2

T1

T3

Each phase has a lots of logic state change "1" -> "0" and "0" -> "1"

Phase I (adder)
Phase II (1st range DFF)
Phase III (2nd range DFF)
Previous work: Implementation 2-Ch TDC

1st delay element circuit

SRAM bits

| 0/1 | 0/1 | 0/1 | 0/1 |

LUT Input

LUT Output

Ex, 2-bit LUT

Input signal

Fast MUX network

ALM

LUT

MUX

LUT

MUX

ALM

Fast MUX network

Cin='0'

'L'

DQ

DQ

Cout

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Laboratory Test

Linear

56 Channels Delay

\[ f(x) = 1.02985183114347x + 465.367328487556 \]

\[ R^2 = 0.999750410678288 \]