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Multi-channel time-tagging module for fast-timing Resistive Plate Chamber detectors

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To update associated electronics with fast-timing resistive plate chamber (RPC) detectors, we present here a multi-channel time-tagging module implemented on a low-end and low-power cyclone V FPGA. A key part in each channel has a time-to-digital converter (TDC) in tapped-delay-line (TDL) architecture (built with delay line and associated registers, fine-time encoder, coarse-time counter and look-up-table memory). The firmware implementation employs several techniques, including input-signal reshaping and bubble-noise filtering to deal with GBVS (ground bounce and Vcc sag) effects. It has successfully been tested in all-channel simultaneous operation conditions, with 9.2 to 12.85ps time resolution and full event-detecting efficiency.

Summary

New generation of resistive plate chamber (RPC) has been proposed to equip two of the high η muon stations in view of the high-luminosity large hadron collider (HL-LHC) phase. The RPC should be instrumented with precise timing readout electronics. The system requires multi-channel readout and time-tagging electronics with low power consumption. This has led us to develop a new readout board including a time-tagging module. The readout board incorporates two multi-channel front-end readout ASICs followed by a low-cost and low-power Cyclone V GT FPGA. The time tagging is performed by the FPGA based on multi-channel time-to-digital converters (TDC) to fulfill the following requirements: full event-detecting efficiency, up to 16-channal simultaneous measurements, 30ns dead time and less than 60ps RMS (root mean square) time resolution.

The time-tagging module via FPGA firmware implementation has 48 channels: 46 for input signal tagging, one for external trigger signal tagging and another for reset signal tagging.

One key part of the module is the TDC in each channel. To implement it, we have adopted the tapped-delay-line (TDL) architecture (built with delay line and associated registers, fine-time encoder, coarse-time counter and look-up-table memory). For operation with a 400-MHz clock, the delay-line consists of over 500 delay elements, each connected to pipeline D-type flip-flop (DFF) registers. It operates in two phases. In the first (within a clock cycle), one single input signal's transition edge can successively toggle hundreds of delay-elements as it propagates in the delay line. In the second phase (the two following cycles), the DFF register could toggle simultaneously at the clock's rising edge. This simultaneous large-scale toggling in a small area could induce ground bounce and Vcc sag (GBVS). The GBVS effect is more marked in the low-power and narrow-wiring FPGA. Furthermore, for simultaneous operation of TDC channels, the resulting GBVS is a source of interferences, which corrupts the delay elements'states (called bubble noise) and temporally slows down the signal transition time (due to power supply voltage fluctuations). Consequently, this degrades the accuracy of time-tagging measurements.

To deal with this issue, firstly we use a signal-reshaping technique in the delay line implementation: to reshape input signal pulse with an edge-detecting logic followed by a DFF. Secondly we propose a bubble-noise-filter-based encoder to detect the first transition bit and to distinguish between signal and noise according to signal' s transition pattern.

Each channel includes a coarse time counter for extending measurement range, and a look-up-table memory for fine-time-to-digital conversion. For an input tagging channel or the trigger one, it gives the measured signal's timestamp. The reset tagging channel employs a TDC to detect extern reset signal from the system,

for a timing precision of system synchronization below 20 ps. The final signal's timestamp is obtained by subtracting the measured timestamp by the reset one.

The time-tagging module has successfully been tested in all-channel simultaneous operation. It gives a tagging time resolution of 9.2 to 12.9ps RMS, with full event-detecting efficiency. The next system test at CERN has been scheduled.

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