Contribution ID: **24** Type: **Poster**

# A High Speed Programmable Analog-to-Digital Conversion System Based On System in Package

*Tuesday 3 September 2019 17:20 (20 minutes)*

The nEXO project is designed to search for the 0vββ process of 136Xe. It requires high reliability and small volume in the readout electronic system. This research is to improve the integration and the reliability of the circuit. The core chip of the system is a highly integrated programmable chip based on SIP which include two ADC dies and a FPGA die. The complete system is constructed by adding the corresponding circuit, and it has the functions of dual-channel high-speed data sampling, data assembly, communication, and real time data processing.

## Summary

The search for the 0vββ process is one of the most important experiments in the field of neutrinos. The purpose of Enriched Xenon Observatory (EXO) experiment is to find the 0vββ process of 136Xe. EXO-200TPC is the prototype detector of EXO experiment. Since June 2011, 136Xe has been discovered for the first time. On the basis of EXO-200TPC, the EXO cooperation group is actively promoting the nEXO project and continuing the search for the 0vββ process of 136Xe. nEXO experiment puts forward high requirements for the reliability and volume of electronic design. The purpose of this research is to improve the integration and the reliability of the circuit design by packaging two ADC dies and a domestic FPGA die together based on SIP technology. The high-speed ADC chip and the domestic FPGA chip are both developed in China, and they are both very high performance chips. We first made a testing board to make sure that the domestic FPGA has the ability to receive the 14 channels'high speed data stream. And it was confirmed that the ISERDES of the domestic FPGA is qualified for this data receiving task. And then here's some details of how to package these two high-performance chips into a small one, we used eight layer substrates with the material of BT HL832NX, and interconnected in any layer of the structure. The flip chip pad pitch is 203um while the diameter of the flip chip pad is 150um. Then the methods of the packaging are SMT + FLIP CHIP + WIRE BONDING. The size of the final module is 35mm*35mm, and the thickness is 2.9mm. With this chip as a core, a complete front-end data sampling system can be constructed by adding the Front-End amplifier Chip (FEC), the back-end serial communication network port and the corresponding power supply module. The details of the system and performance test result will be contained in the article. Overall, compared with traditional PCB design, the SIP-based design reduces the volume of the whole system and increases the reliability of the circuit design. From this research, first we provide a new design way of the readout system for nEXO, and second we can get a highly integrated high speed programmable ADC chip which can be used in any other situations.

**Primary authors:** Mr JIN, Ruyi (Institute of High Energy Physics); Dr HU, Jun (Institute of High Energy Physics); Dr JIANG, Xiaoshan (Institute of High Energy Physics)

**Presenter:** Mr JIN, Ruyi (Institute of High Energy Physics)

**Session Classification:** Posters

**Track Classification:** Programmable Logic, Design Tools and Methods