Methods for Clock Signal Characterization using FPGA Peripherals

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Motivation

Characterization of clock signal parameters is typically done using off-the-shelf measurement equipment. For specialized ASIC testing applications, which demand multi-channel measurements while minimizing measurement time or have a need for real-time dynamic measurements, two alternative measurement schemes were developed.

Static Signal Characterization Method

- FPGA PLL multiplies and phase-shifts DUT reference clock
- Clock signal under measurement is sampled by synchronous delay line
- Accumulators digitize probability of observing clock signal as 0 or 1
- Repeated for multiple sampling clock phases: Equivalent Time Sampling

![Figure 1: Architecture for Static Signal Characterization](image1)

- Offline processing of reconstructed time series
- Estimation of time offset and jitter for each clock edge
- Calculation of signal frequency, phase (skew), duty cycle and clock jitter
- Picosecond-level measurement resolution
- Uncalibrated edge time estimation error below 62 ps on Xilinx Virtex 7
- Uncalibrated rms jitter estimation error below 20%
- Calibration of PLL phase step size can be used to improve accuracy

![Figure 2: Clock Skew Estimation Error](image2)

Dynamic Signal Characterization Method

- Radiation effects in clock synthesis ASICs can produce phase transients
- Direct triggering on phase not possible with off-the-shelf test equipment
- High-speed data receivers in modern FPGAs allow bypassing CDR
- Direct sampling of clock signals with multiplied reference clock possible
-Deserializer operates at 10 Gbit/s: 100 ps TDC resolution
- Parallel data words presented to FPGA fabric at low clock speed
- Triggering and data acquisition implemented in generic FPGA fabric

![Figure 3: Architecture for Dynamic Signal Characterization](image3)

- Implemented using Xilinx Virtex 7 FPGA & GTX receivers @ 10.24 Gbit/s
- Phase detection and triggering implemented as VHDL core
- Dead-time free triggering on 100 ps phase transients / glitches
- TDC INL better than 52 ps, DNL below 15 ps

![Figure 4: Captured Example Phase Transient](image4)

Summary

- Two FPGA-based methods for clock characterization presented
- Both methods implemented and characterized for performance
- Can eliminate dependency on dedicated measurement equipment
- Flexible architecture allowing multi-channel measurement systems
- Successful application in test campaigns and ASIC production testing
- Performance expected to improve with future FPGA generations

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