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Methods for Clock Signal Characterization using FPGA Peripherals

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Reliable measurement of clock signal parameters is important in precise-timing applications. Such parameters include frequency, phase, duty cycle and channel-to-channel skew. Especially in applications in which test time for multiple channels is a significant factor, efficient parallelization of measurements is crucial, while often coming with significant extra cost. This work presents an approach to characterizing clock signal parameters using off-the-shelf FPGA evaluation hardware.
Approaches for both static measurements (steady-state behaviour) as well as dynamic measurements are presented. Both presented measurement concepts are applied in practice and their achieved performance is presented.

Summary

The dynamic clocking architecture of modern FPGAs combined with their flexible reconfiguration options allows using them to implement high-performance measurement systems replacing commercial test equipment without requiring complex external circuitry. This work presents two methods that can be used to characterize clock signals.

The first method presented allows estimation of static signal parameters for clocks synchronous to a reference clock. It implements an equivalent-time sampling concept by dynamically reconfiguring FPGA PLLs to acquire high-resolution measurements of signal phase (skew), duty cycle and jitter.
The DUT clock signals are sampled using a phase-shifted clock by fabric flip-flops, producing single-bit-quantized outputs. By collecting multiple samples, a measure of probability of the clock signal being high is estimated for each sampling phase offset. The implemented design using the PLLs available in Virtex 7 FPGAs achieves sampling phase increments of 28 ps, dictating the fundamental measurement resolution. By post-processing the acquired data, the temporal resolution can be improved further and additional information about clock jitter can be extracted. Due to the simple architecture and low resource requirements, multiple channels can easily be implemented in a single FPGA.

The second method presented in this work allows transient phase measurements on arbitrary clock signals. It is shown how the Multi-Gigabit transceivers of Virtex-7 FPGAs can be used for this application. Configuring the integrated GTX receivers in a mode where the deserializer operates from a fixed reference frequency (without a CDR being engaged) allows deserializing clock signals with high oversampling ratios, allowing for precise phase measurements without dead time. Multiple measurement channels can be implemented by simply using multiple hardware GTX instances without sacrificing resolution. One of the advantages of such an implementation is that data acquisition can be deterministically synchronized to other FPGA-based components of a test system, which is hard to achieve with external test equipment. FPGA logic can be used to control data acquisition of these signals, for example triggering on phase transients can be done when characterizing PLL circuits. By implementing a modified processing logic in the FPGA fabric, the GTX receivers can also be easily repurposed to operate as a TDC. With the Virtex 7 FPGA series receivers supporting bit rates up to 10.51 Gbit/s, time resolutions of 95 ps can be achieved with very good linearity and without any dead time.

The presented methods were integrated into the test system used for the lpGBT ASIC. The method for static determination of clock signal parameters is used in production testing, where it allows to measure the char-

acteristics of all 28 ASIC clock outputs at the same time and can test them for expected functionality and performance. The dynamic phase measurement implementation was used during two SEU test campaigns and facilitated detection of small phase transients that would have otherwise been detected only with dedicated high-speed test equipment.
Both methods will be discussed at the workshop and the experimental results presented.

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