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The Firmware for the European Spallation Source Cavity Simulator

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The Cavity Simulator reproduces the behavior of superconducting cavities and high power amplifiers used in the medium and high beta sections of European Spallation Source (ESS) linac. The device is foreseen to be used for tests and development of the ESS's LLRF control system. High-performance Xilinx Kintex Ultrascale FPGA runs dedicated firmware, which performs all calculations including the simulation models. The firmware is also responsible for device control and communication. This contribution presents the general overview of the Cavity Simulator's firmware together with simulation and measurement results.

Summary

The Cavity Simulator reproduces the behavior of superconducting cavities and high power amplifiers used in the medium and high beta sections of the European Spallation Source (ESS) linac. The simulated phenomena include, but are not limited to: klystron bandwidth and non-linearity, the influence of the power supply ripple, cavity dynamics, beam loading, Lorentz force detuning, microphonics, as well as mechanical modes. The device is foreseen to be used for tests and development of the ESS's LLRF control system.

A digital FPGA circuit executes the simulation algorithm. However, the Cavity Simulator operates on RF and analog signals. Therefore a dedicated frontend and set of data converters are used. The input RF signals are first down-converted to an intermediate frequency and then sampled by high-speed ADCs. Vector modulator circuits generate the RF output signals. Additionally, the device is equipped with RF reference, Local Oscillator (LO) and clock signals generation modules.

High-performance Xilinx Kintex Ultrascale FPGA runs dedicated firmware, which performs all calculations including the simulation models. The firmware is divided into three blocks: hardware interface, model and communication. The first part is responsible for the connection to the data converters and other circuits used. It also converts the signals from the ADCs into an IQ complex vector format, which is used for the signal processing. The cavity model consists of six tunable IIR filters that simulate the transfer function of all pi-modes. Other elements of the model detune the filters. The device mimics the piezo actuator used for fine-tuning of the cavity resonance. The piezo simulation includes modeling of the hysteresis, based on a Dahl model. The firmware architecture is optimized for the shortest possible processing time. So are the selected algorithms and their implementation.

The firmware is also responsible for device control and communication through an Ethernet network or USB interface. These functions are realized by a Micro-Blaze softcore processor, which communicates with other blocks through the AXI bus.

This contribution presents the general overview of the Cavity Simulator's firmware together with simulation and measurement results.

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