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Readiness of the ATLAS Tile Calorimeter link daughterboard for the High Luminosity LHC era

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The Daughterboard (DB) is the readout link and control board that interfaces the front-end and off-detector electronics for the HL-LHC of the the ATLAS Tile Calorimeter. The DB sends high-speed readout of digitized PMT samples, while receiving and distributing configuration, control and LHC timing. A redundant design, Xilinx SEM, TMR, FEC and CRC strategies minimize single failure points while withstanding single-event upsets and damage from minimum ionizing and hadronic radiation. We present the current results of the performed TID, NIEL and SEU tests, aiming to demonstrate the readiness of the Daughterboard to withstand the radiation requirements imposed by the HL-LHC.

Summary

The Phase-II upgrade plans for the ATLAS central hadronic Calorimeter, the Tile Calorimeter, facing the High Luminosity LHC (HL-LHC) era includes approximately 1024 radiation tolerant readout link and control boards (Daughterboards) that will provide full-granularity digital data to a fully-digital trigger system off-detector through multi-Gbps optic fibers. Four commencial SFP+ modules handle 4x9.6 Gbps uplinks driven by two Kintex Ultrascale+ FPGAs and 2$\times$4.8 Gbps downlinks driven by two GBTxs. The Daughterboard design minimizes radiation-induced errors and enhances data reliability by:
- embracing a fully double redundant design,
- using CERN radiation hard GBTx ASICs and Kintex Ultrascale+ FPGAs,
- implementing Triple Mode Redundancy in the FPGA firmware,
- employing the Xilinx Soft Error Mitigation (SEM) to correct for configuration memory SEEs,
- using CRC error verification in the redundant uplinks while FEC is handled by the each GBTx in each downlink.

We have performed TID, NIEL and SEU radiation tests in order assess the radiation tolerance strategies followed in the design and to qualify the Daughterboard for the HL-LHC requirements according to the ATLAS policy on radiation tolerant electronics. Over the HL-LHC lifetime, the Daughterboard positioned on the area most exposed to radiation will have to withstand 23.57 kRad of Total Ionizing Dose, a total Non-Ionizing Energy Loss corresponding to 1.12655xE12 - 1 MeV equivalent neutron fluence, and seamlessly run and recover from any single event upset and single event latch-up for a fluence of 1.35987xE11 protons per cmˆ2. We present the current results of the radiation tests performed to demonstrate the readiness of the Daughterboard to withstand the radiation requirements imposed by the HL-LHC, and the new strategies derived to mitigate and minimize the undesired SEU effects seen during the tests.

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