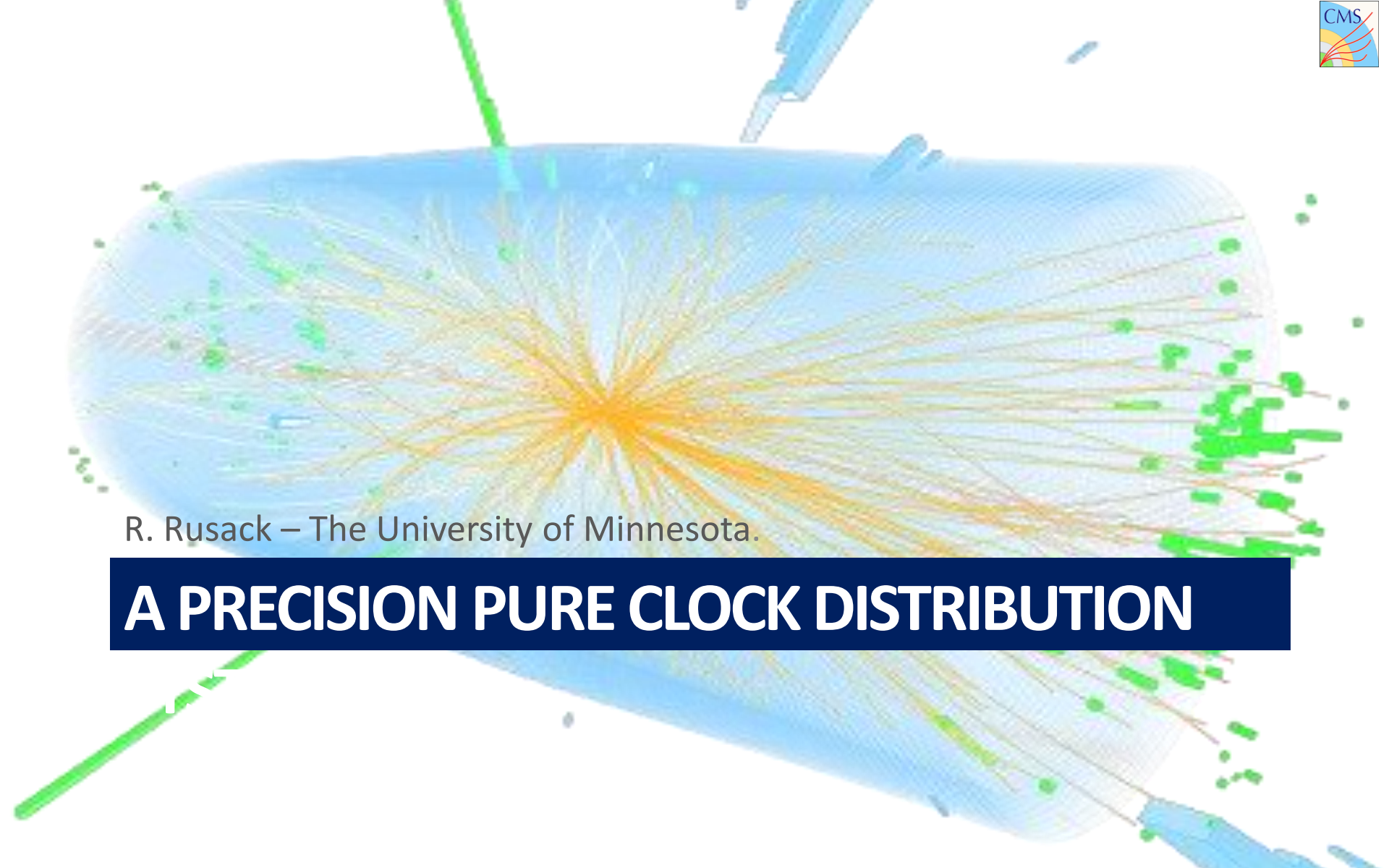


R. Rusack – The University of Minnesota.

A PRECISION PURE CLOCK DISTRIBUTION

Collaborators

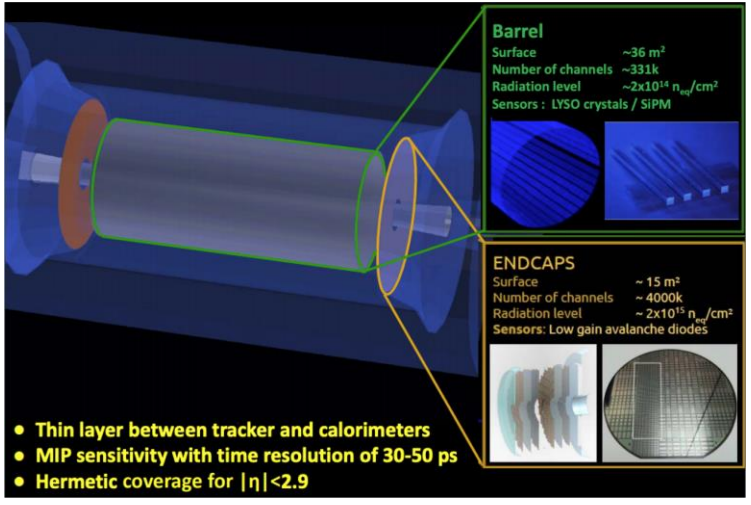
J. Brashear, E. Frahm, S. Jain, R. Rusack, R. Saradhy
The University of Minnesota

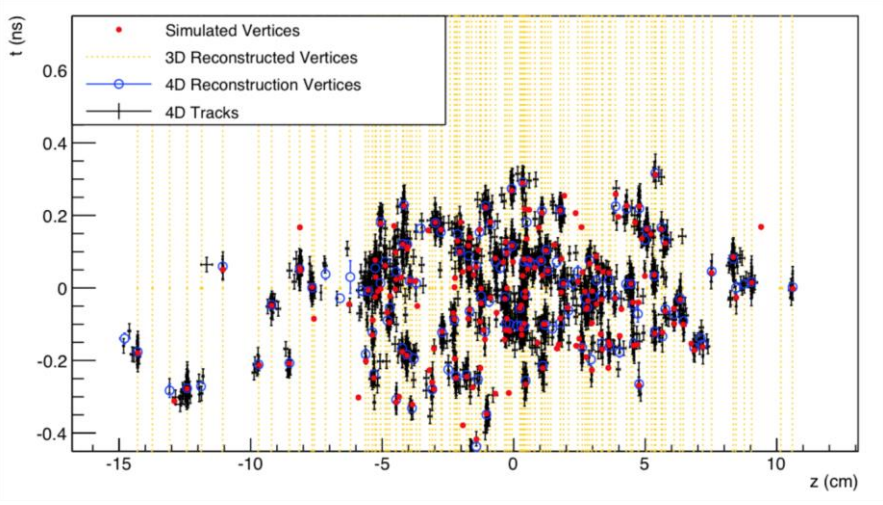
N. Loukas
The University of Notre-Dame

P.-A. Bausson, M. Besançon, Ö. Sahin
IRFU, CEA, Université Paris-Saclay

The Problem to be Solved

- The CMS detector is being upgraded with new detectors which measure the time of the arrival of particles with precision of ~30 ps.
  - Mip Timing Detector (MTD), ECAL and HGCAL.
- 10,000 clocks synchronized to less than ~10 ps needs to be distributed to all of them
- Clock distribution is ~80 m from the detector.
- Detector components are up to 10 m apart.
- Light travels 3mm in 10 ps in vacuum.

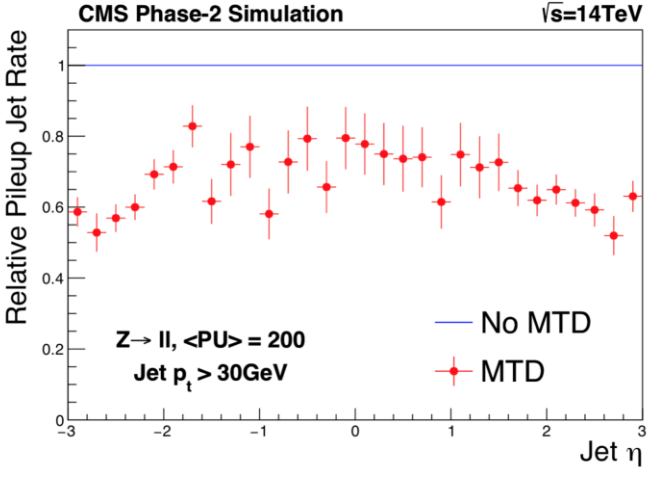




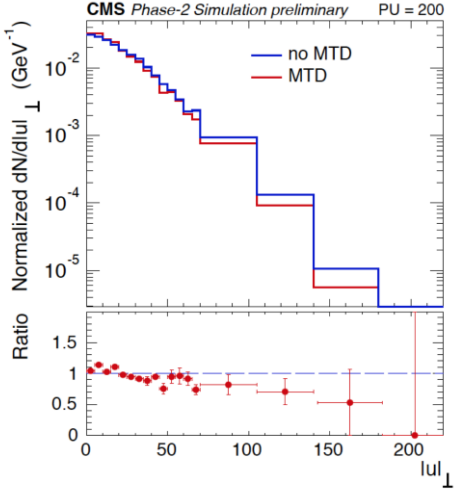
Physics Motivation

- Mitigate effects of 200 interations in a bunch crossing.
  - Improve missing p_T , b tagging, jet energy resolution etc.
- Particle identification in nuclear collision events in heavy-ion running.

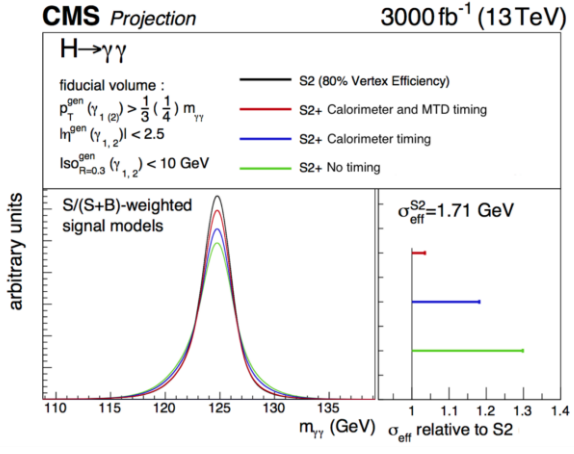
Pile-up Jet rate



Missing p_T resolution and tails



Restores Run 2 performance in H →γγ



Figures of Merit

- We need to identify by timing which tracks or energy deposits are associated with a vertex and reject those that are out of time. Overall hit resolution is 30 ps.
  - All detector signals in need to be referenced against a clock that is aligned to better than 10 ps. (TIE_{SS} < 10 ps)
- Low phase noise at high frequency in a clock for data link stability. (TIE_{MS})

In principle with data it is possible to correct for low frequency wander using particles in the detector in intervals of 1 second.

~10,000 precision clocks distributed to CMS detectors at 320 MHz, 160 MHz & 40 MHz.

Pure Clock Demonstrator System

Concerns:

- A clock distribution system that uses clock recovery from the encoded downlink control signal is a complex network with multiple frequency modifications, encoding and decoding in the FPGAs and the LpGBT, has various connectors and media (ATCA backplane, optical fibers etc.) and may not meet the requirements of CMS.
- Jitter cleaning PLLs in different clock branches will partially move noise power randomly, from high frequency to low frequency and introduce noise in TIE_{SS}.

- Demonstrator system to investigate what can be achieved in a pure clock distribution.

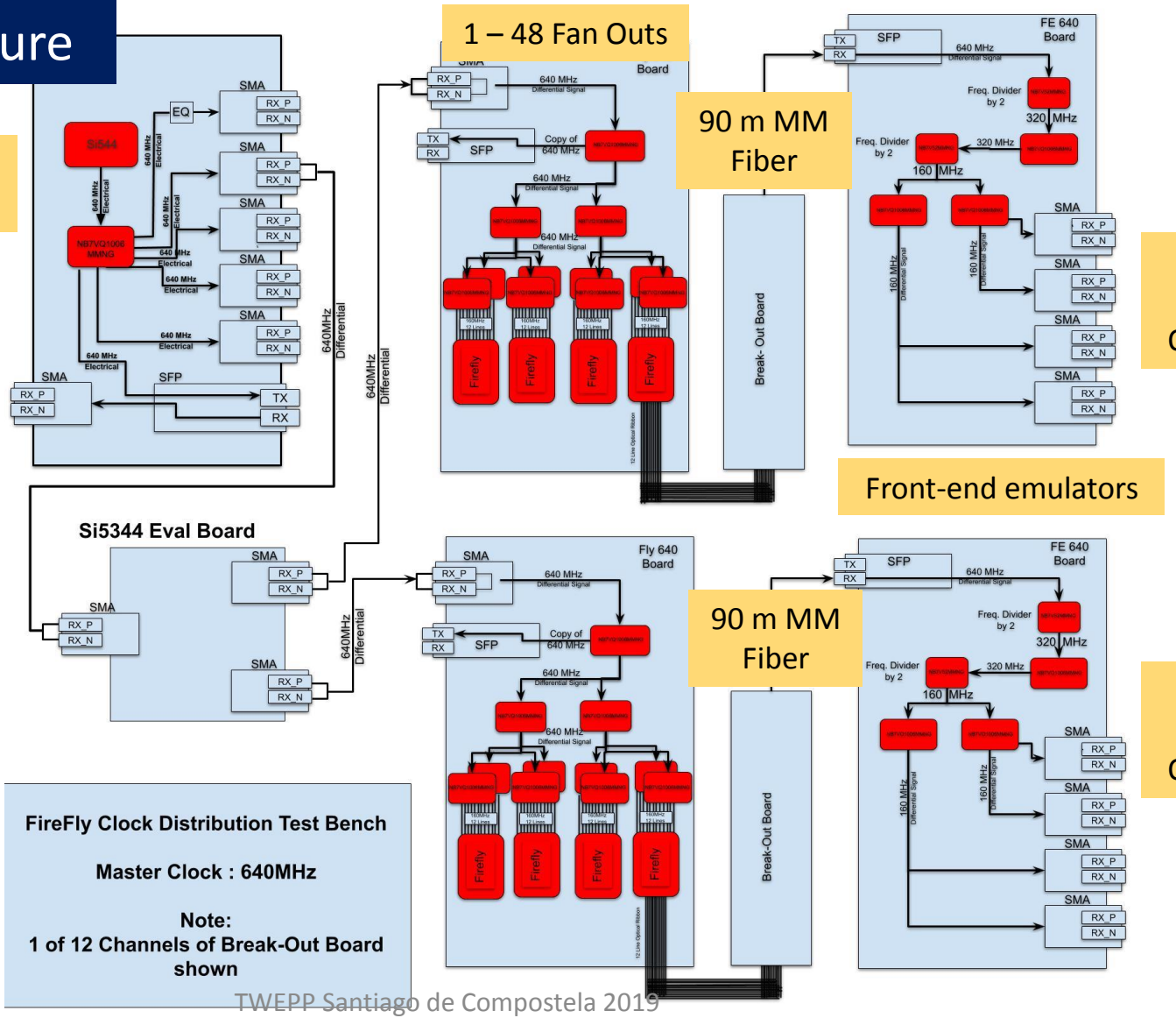
Overall design philosophy:

- *Use modern high-speed RF components.*
- *Make it realistically scaleable*
- *Explore different distribution techniques.*

Overall architecture

Custom 640 MHz clock board

Input here to alternative clock sources.



Design

- All boards are custom boards.
  - PCB material – medium quality with a dissipation factor of 0.006.
  - Used microstrip traces on the top layer, avoiding vias for the high performance signals.
  - Inter-board electrical signals are on differential pairs of SMA connectors.
  - Optical signals transmitted with 12-channel Firefly_TX, alternated 6 in-phase with 6 out of phase by 180 degrees.
  - Optical signals received with SFP+ and VTRx.
  - Pure clock signals transmitted at 640 or 160 MHz.
    - Investigate frequency division by two (or 4) at the destination to reduce phase noise from imperfect waveform duty cycle.
  - Use mid-range RF quality components (~10 GHz) to generate, fanout and divide down the signals.
  - Design with sufficient fanout to be realistic for an experiment. 1 - 1000
  - Measure phase noise and TIE_{ss} between two ends of independent branches.

RF Components

ON Semiconductor Fanout: NB7VQ1005MMNG

Features

- Maximum Input Data Rate > 10 Gbps
- Maximum Input Clock Frequency > 7.5 GHz
- Backplane and Cable Interconnect Compensation
- 225 ps Typical Propagation Delay
- 30 ps Typical Rise and Fall Times
- Differential CML Outputs, 400 mV Peak−to−Peak, Typical
- Operating Range: V_{CC} = 1.71 V to 2.625 V, GND = 0 V
- Internal Input Termination Resistors, 50 Ω
- QFN−24 Package, 4 mm x 4 mm
- −40°C to +85°C Ambient Operating Temperature

ON Semiconductor D-Type Flip-Flop: NB7V52MMNG

Features

- Maximum Input Clock Frequency > 10GHz Typical
- Random Clock Jitter < 0.8ps RMS
- 30ps Typical Rise and Fall Times
- Differential CML Outputs, 400mV peak-to-peak, typi
- Operating Range: VCC = 1.71V to 2.625V with VEE
- Internal 50-ohm Input Termination Resistors
- -40C to +85C Ambient Operating Temperature

Setup time (t_{su}) < 40 ps.
Toggle frequency 12 GHz.

SMA connectors: RF-quality up to 12 GHz

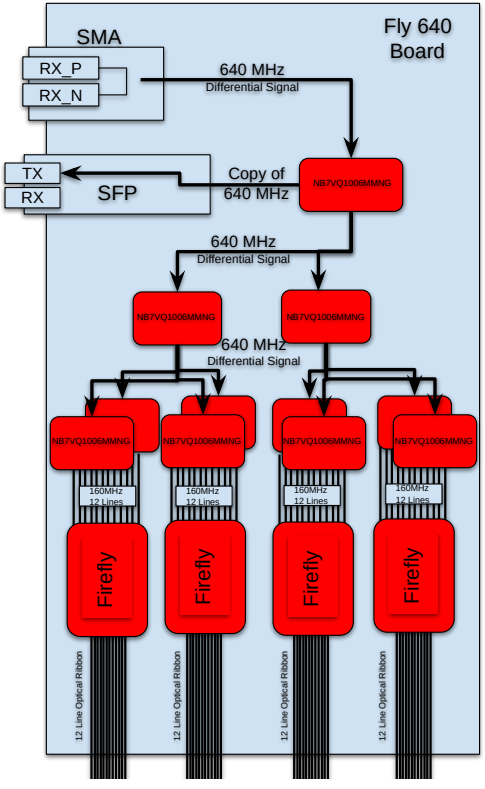
Tests made

1. Distribution of 640 MHz clock with divide by four front-end emulator.
2. Distribution of 160 MHz clock without division SFP – SMA
3. Distribution of 160 MHz clock without division VTRx to SMA.

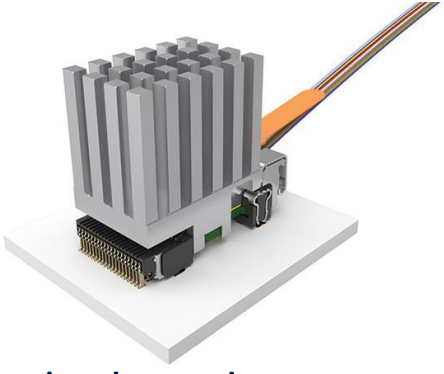
Test equipment:

- 12 GHz Agilent scope and 40 GHz Lecroy SDA 820Zi-B scope.
- Rohde Schwarz FSW67 2Hz to 67GHz Signal and Spectrum analyzer
- Custom Digital Dual Mean Time Difference (DDMTD) circuit
- Microsemi 5275A - Measurement of TIE_{SS}
- Agilent E5052B – Signal and Spectrum analyzer
- And other equipment made available to us by the CERN HPTD lab.

Electrical-to-Optical Fan out board – FLY640.



Two levels of 1 to 6 fanouts drive four Fireflies.
12-Channel O2E drivers.



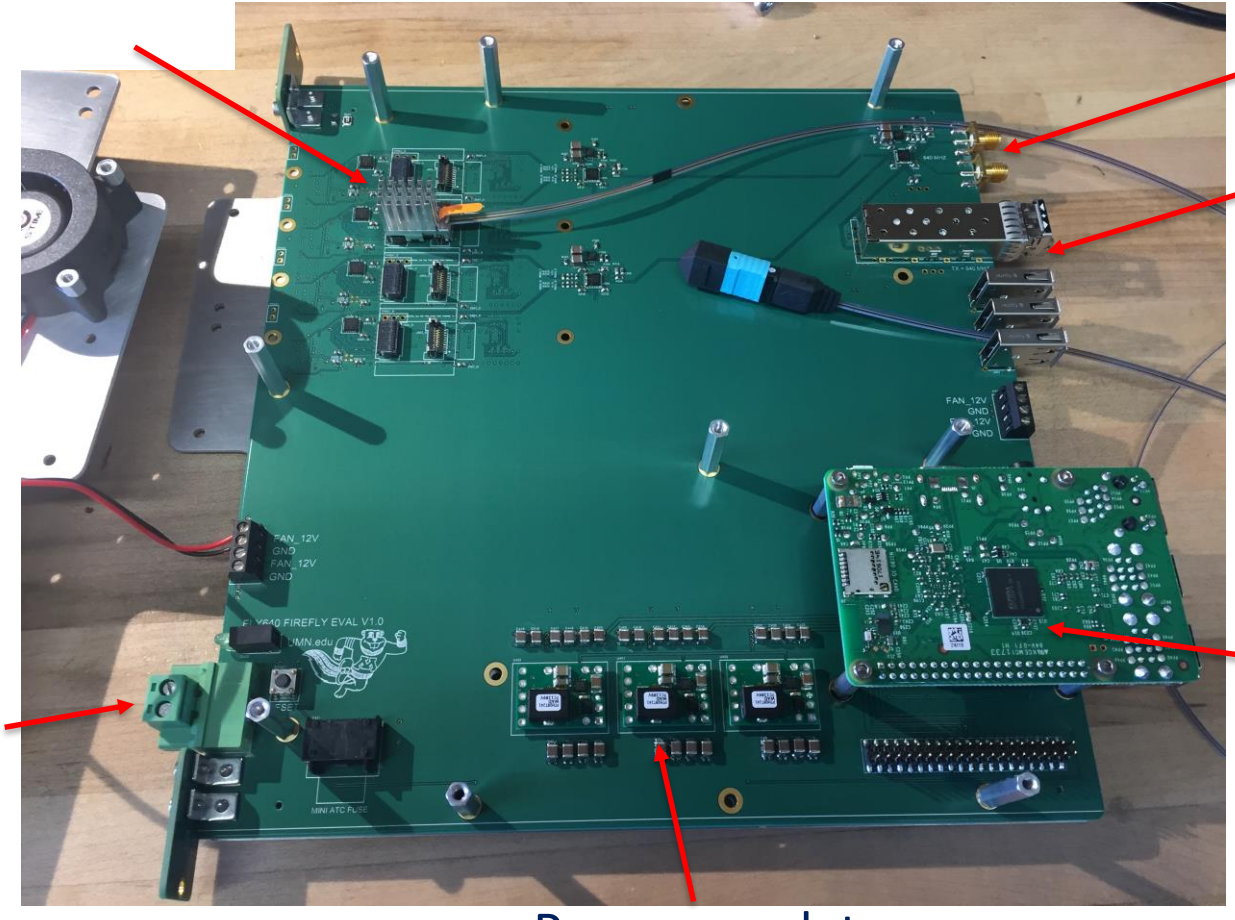
1 to 48 fanout on the board.
Max possible fanout would be to 18 fireflies (1 to 216)

RaspberryPi to control Firefly parameters.
Not used. Default settings used for all tests.

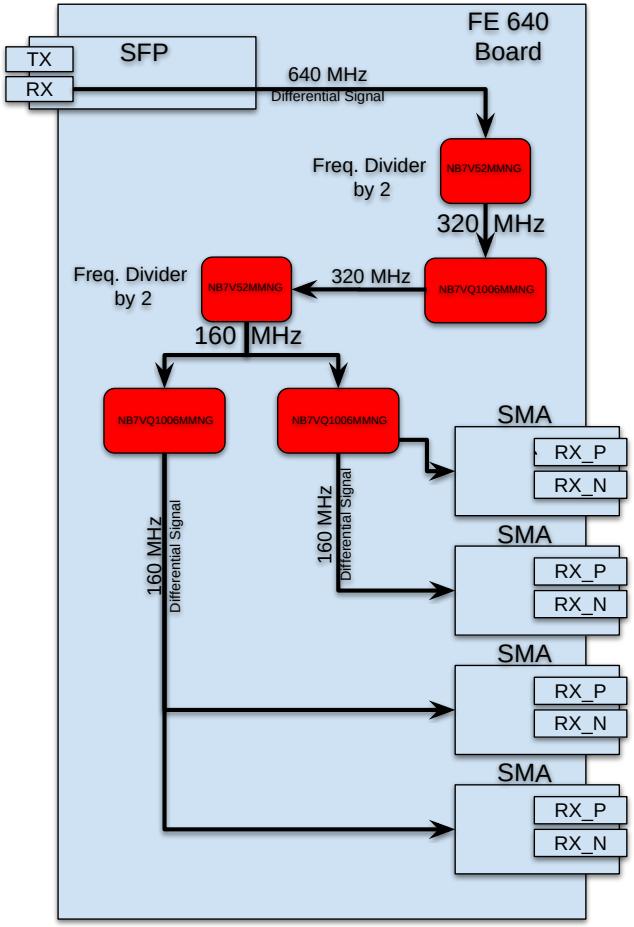
Used in these tests to distribute clock at frequencies from 40 MHz to 640 MHz.

FLY640

Firefly – 12 optical links



Front-End Board Emulator

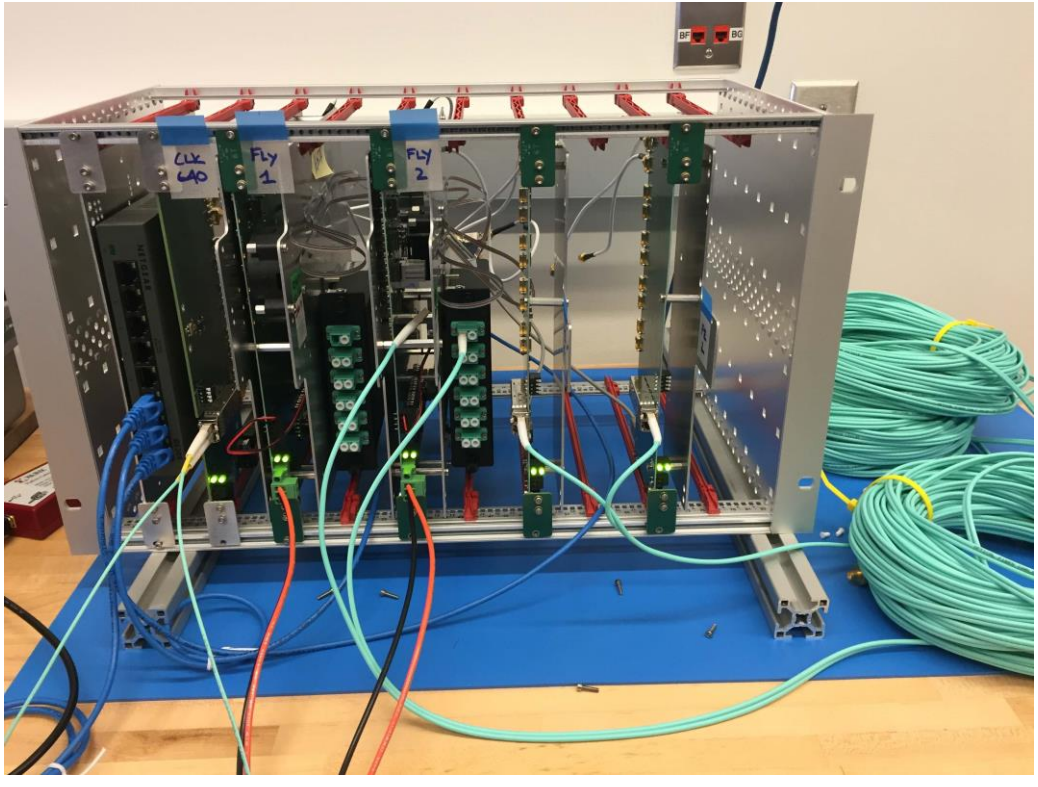


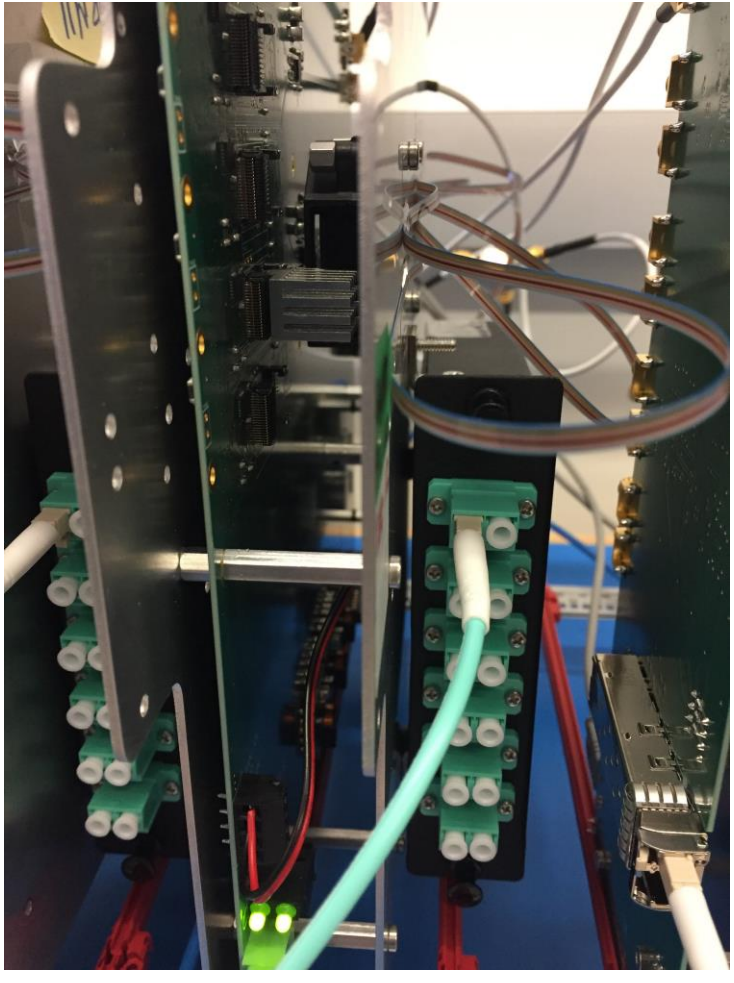
Two levels of 1 – 6 fanout.
Divides clock signal down from 640 MHz to 160 MHz.
Outputs 4 – copies of signals on differential SMAs for the measurement.

All components used in the setup are designed for high speed digital transmission.

The typical RMS jitter of the 1 – 6 Mux and the Divide-by-2 flip-flop is 0.2 ps.

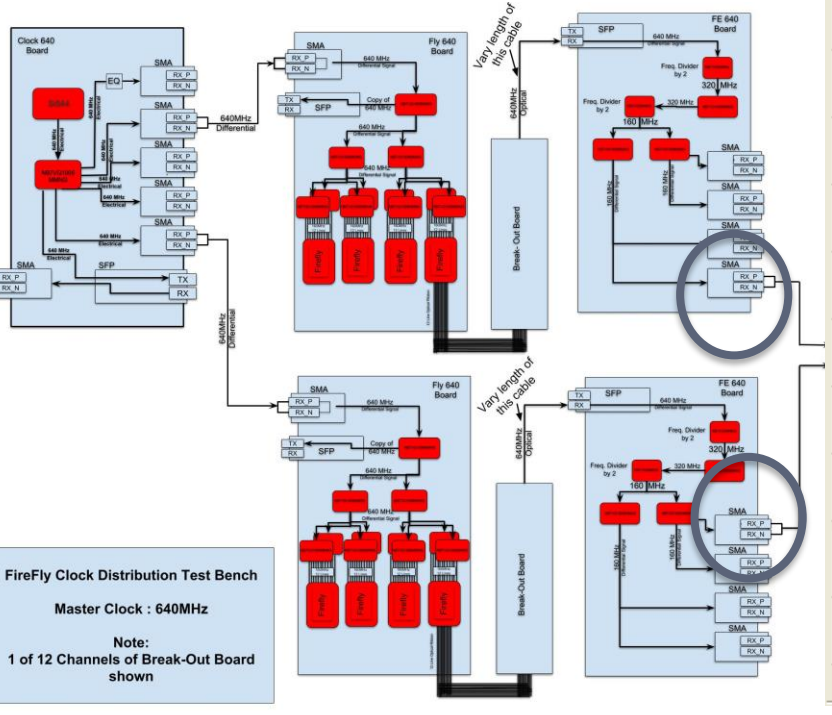
Reality



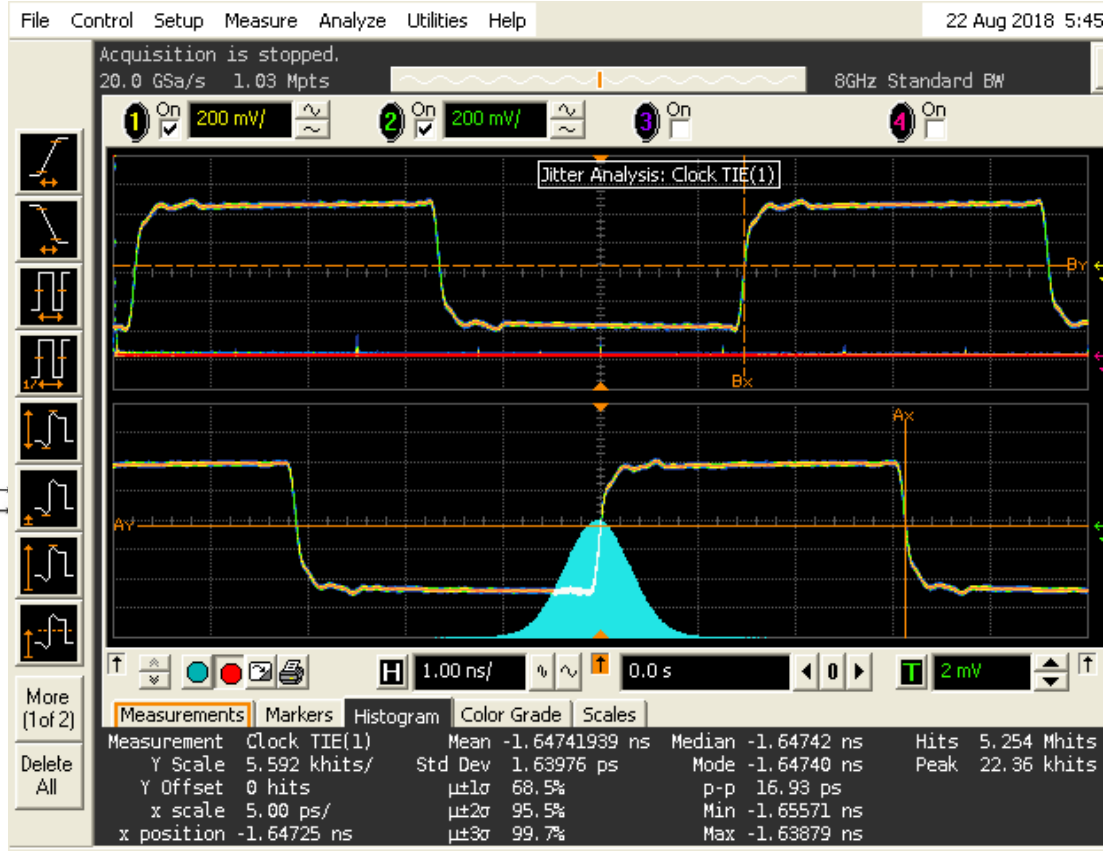


TIE_{SS} of 160 MHz Clock

External Clock mode use the 640 MHz clock. This is the slave-slave mode.

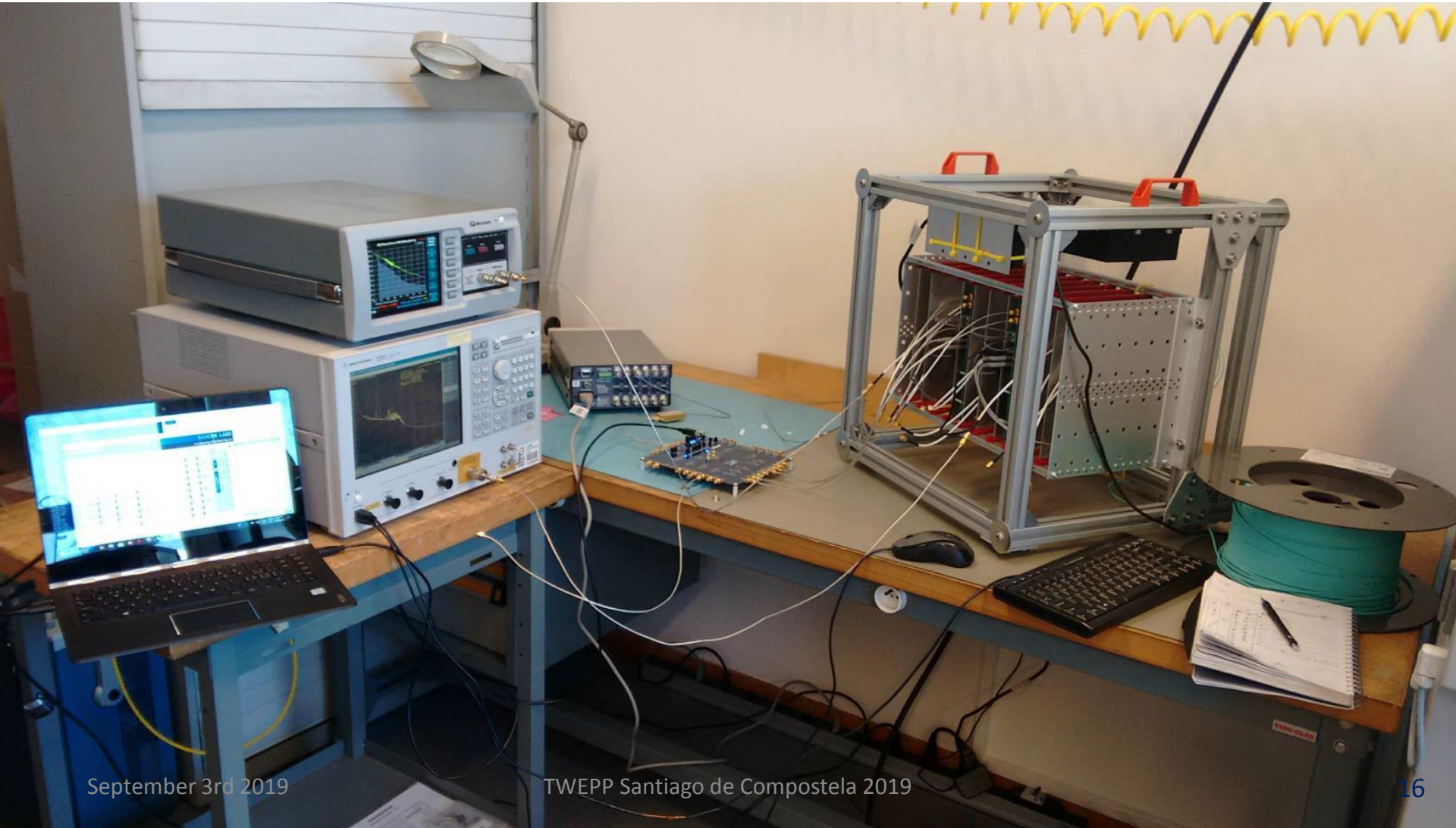


20 Gs/s – 1Mpts --- > 20 kHz



Measure 1.6 ps *TIEss*

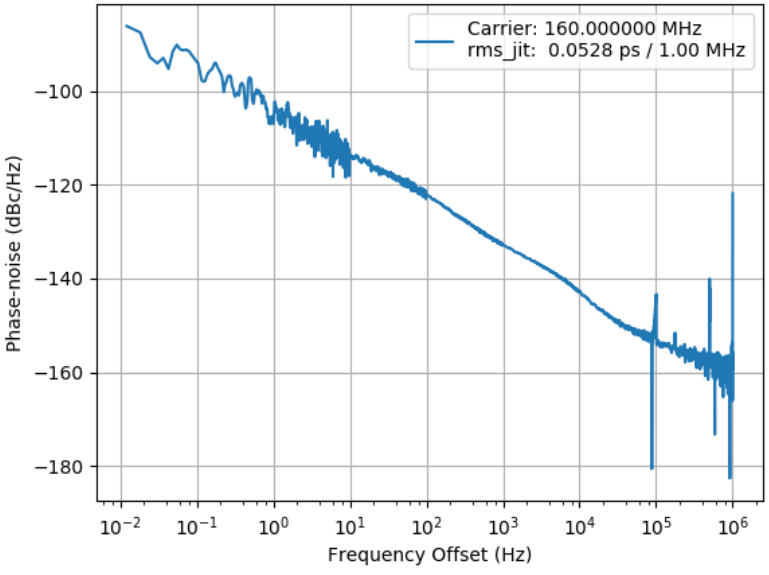
Test Setup at CERN



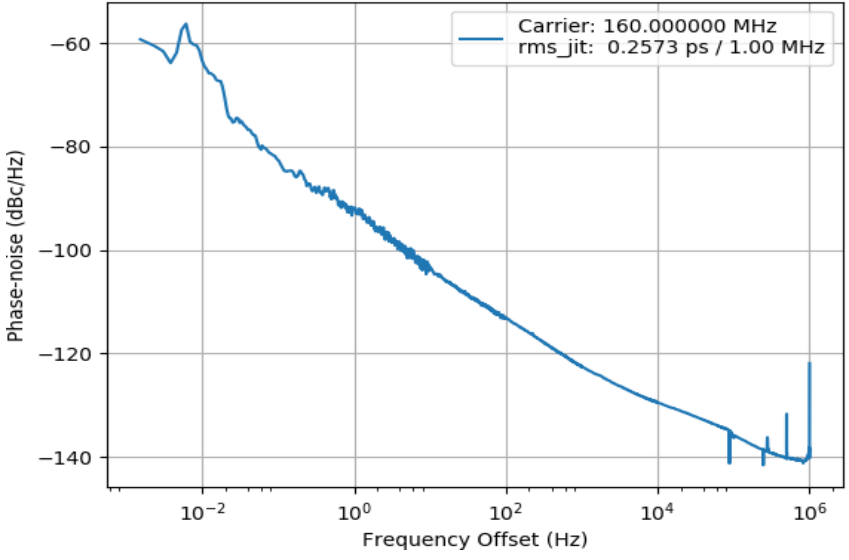
Tests at CERN

Integration between 0.01 Hz to 1 MHz.

TIE_{SS} of copy of clock at input



TIE_{SS} at output of 2 independent branches

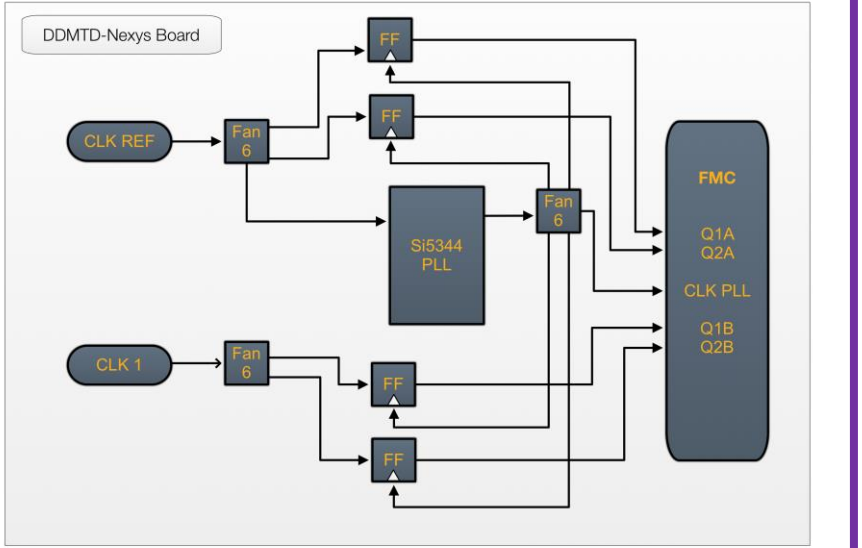


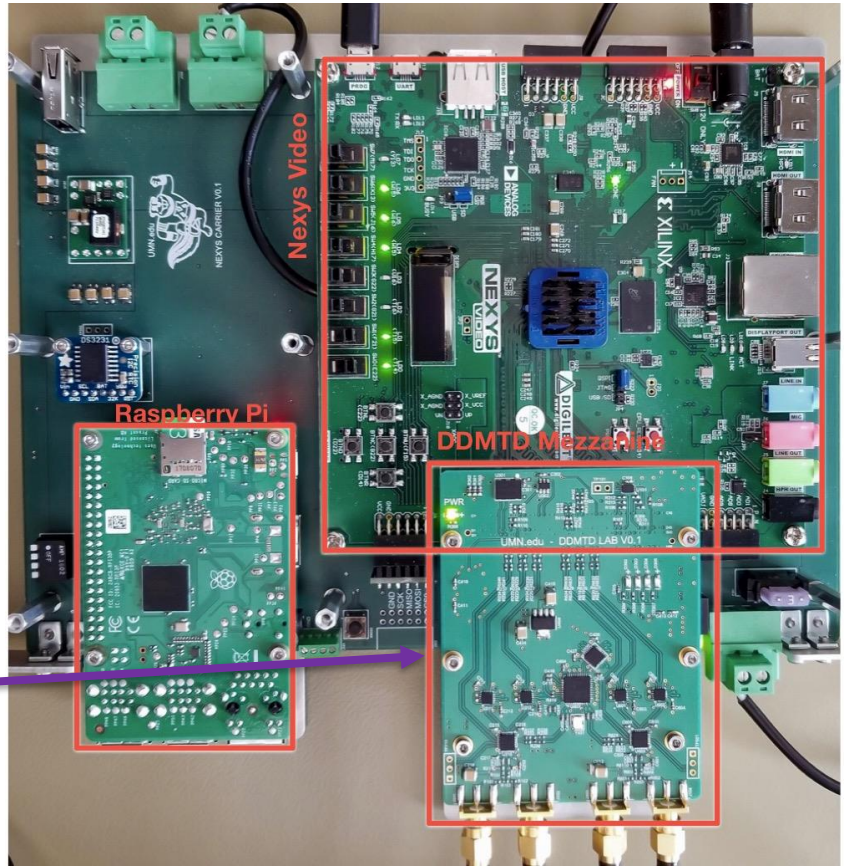
Phase difference noise at source
52 fs

Phase difference noise slave-to-slave
257 fs

Measured at CERN HPTD lab with Microsemi 5275A

Custom DDMTD

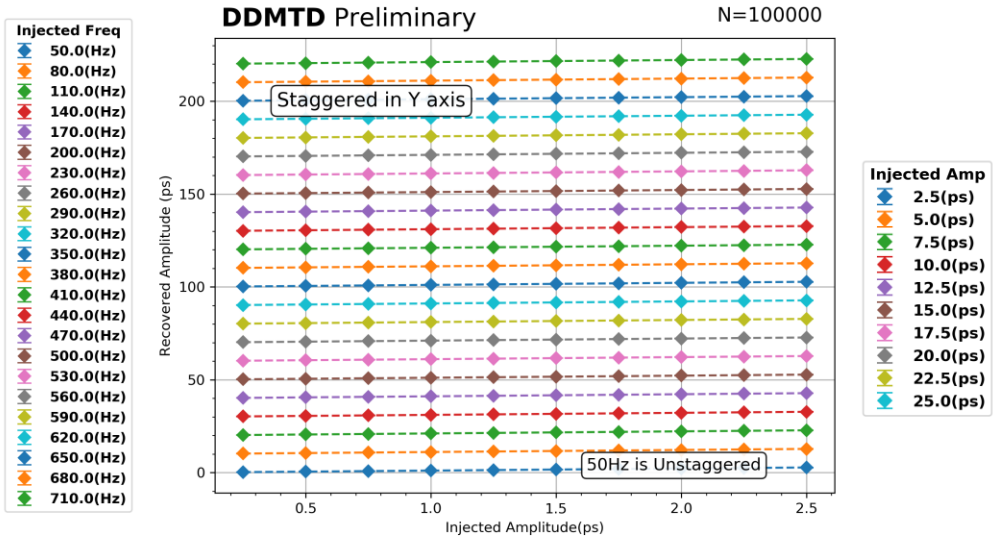


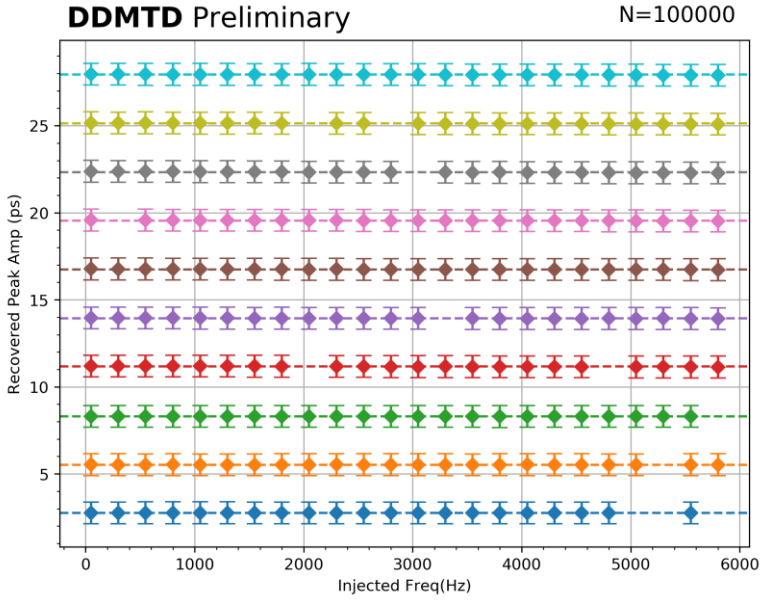


Use Nexsys Video card with Artix-7 FPGA.

DDMTD Performance

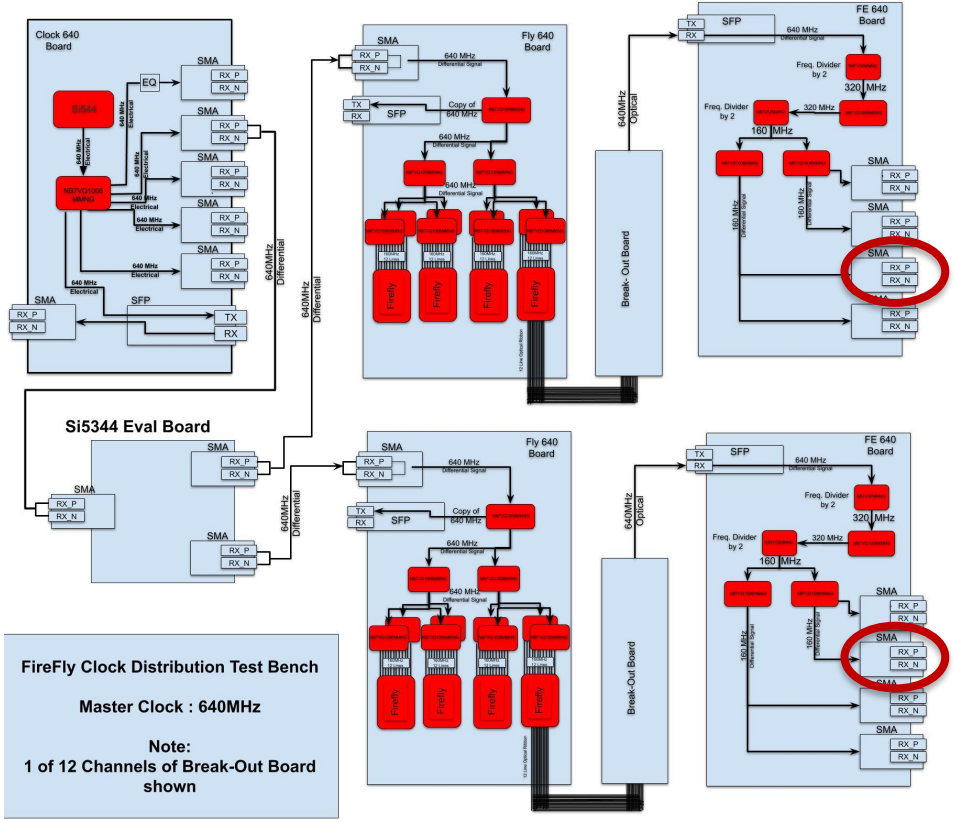
To test performance of DDMTD we injected harmonic phase variations on a 160mMHz Clock and recover frequency and amplitude with DDMTD.



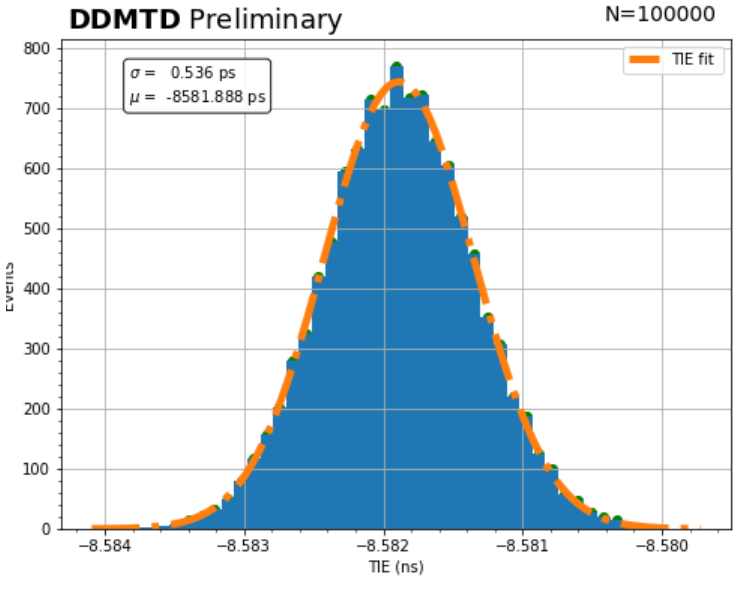


Inject 0.25 ps to 2.5 ps harmonic variations – recover with DDMTD.

DDMTD Measurements



160MHz Clk at N=100000 → up to 1.6kHz

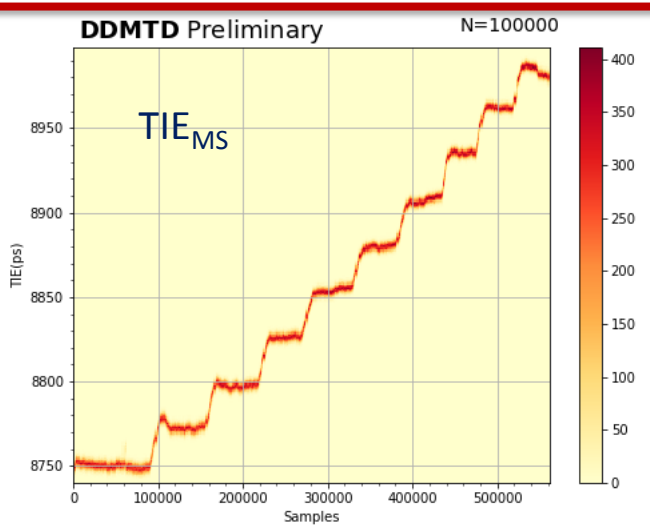


TIE_{SS} = 0.54 ps

Phase variation with temperature

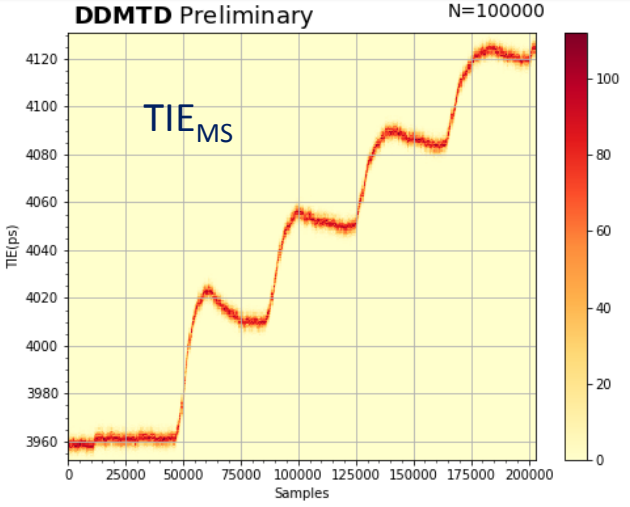
LpGBT and VTRx inside Climate Chamber

- 40 MHz clock distributed by FLY 640 Board
- 28m of optical between FLY640 and VTRx
- LpGBT and VTRx inside Climate Chamber
- Range -30^0 C to +60^{0}C, step is 10^{0}C
- TIE_{MS} 40MHz; clock from LpGBT vs Ref Clock (PLL)
- We observe 25ps for every 10^0 C rise

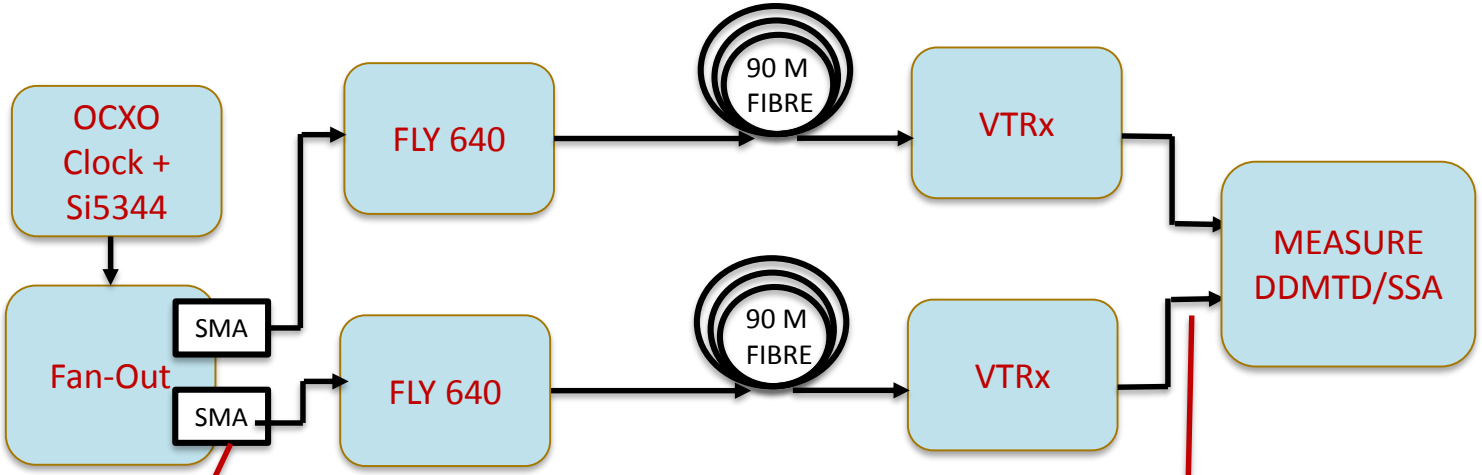


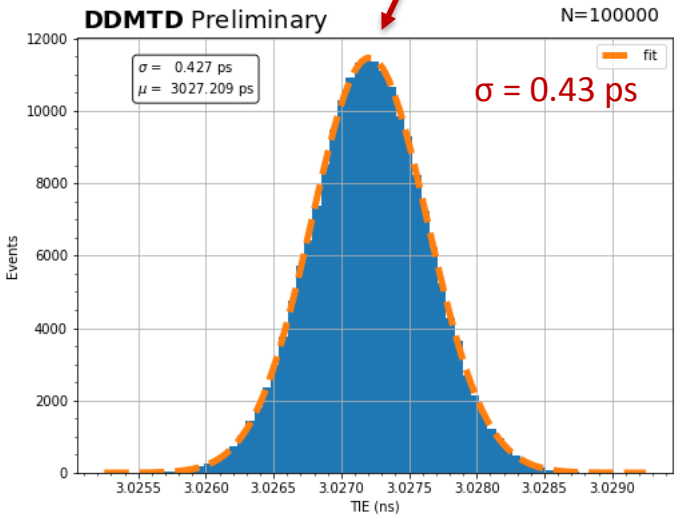
Optical fiber inside Climate Chamber

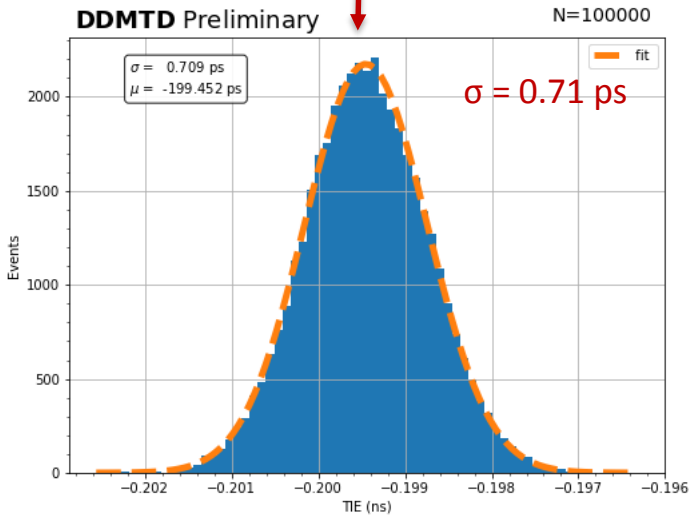
- 40 MHz Clock distributed by FLY 640 Board
- 28 m of MM optical cable inside Climate Chamber
- LpGBT and VTRx kept outside climate chamber
- Range -30^0 C to +60^0 C, step is 10^0 C
- We observe 50 ps step for every 10^0 C



Test with VTRx







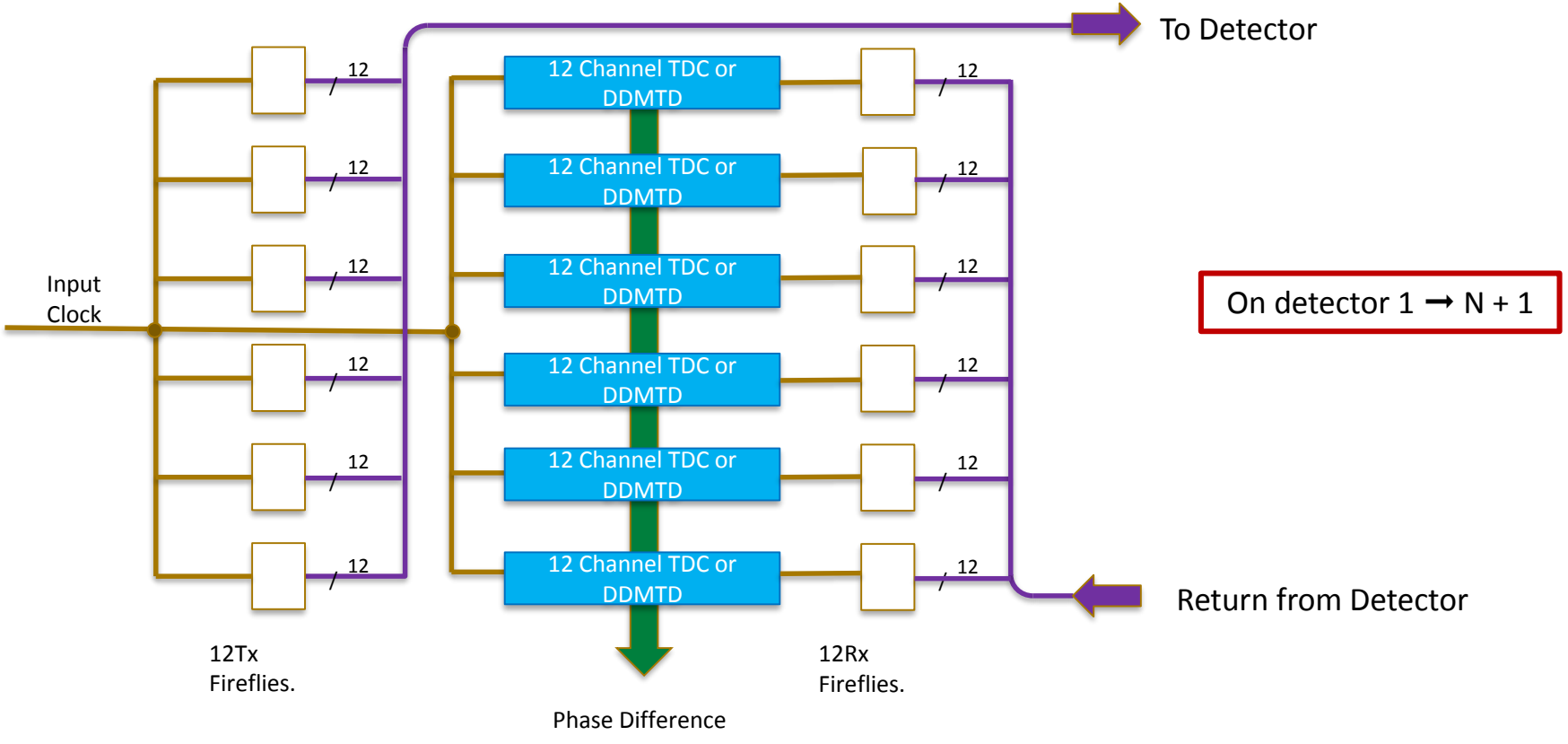
Next Steps

Design clock distribution and monitoring system

Principle:

Distribute clock from off-detector electronics to a 1 → N+1 fanout. Distribute N signals to the FE electronics and send one back to monitor phase shifts in the clock.

PCDM Demonstrator

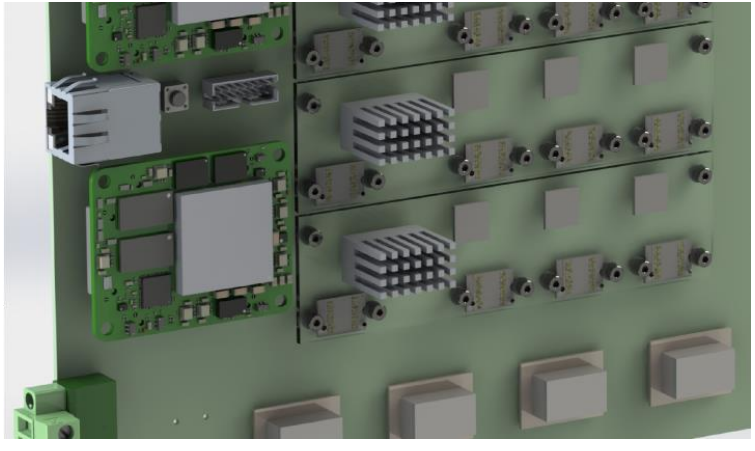


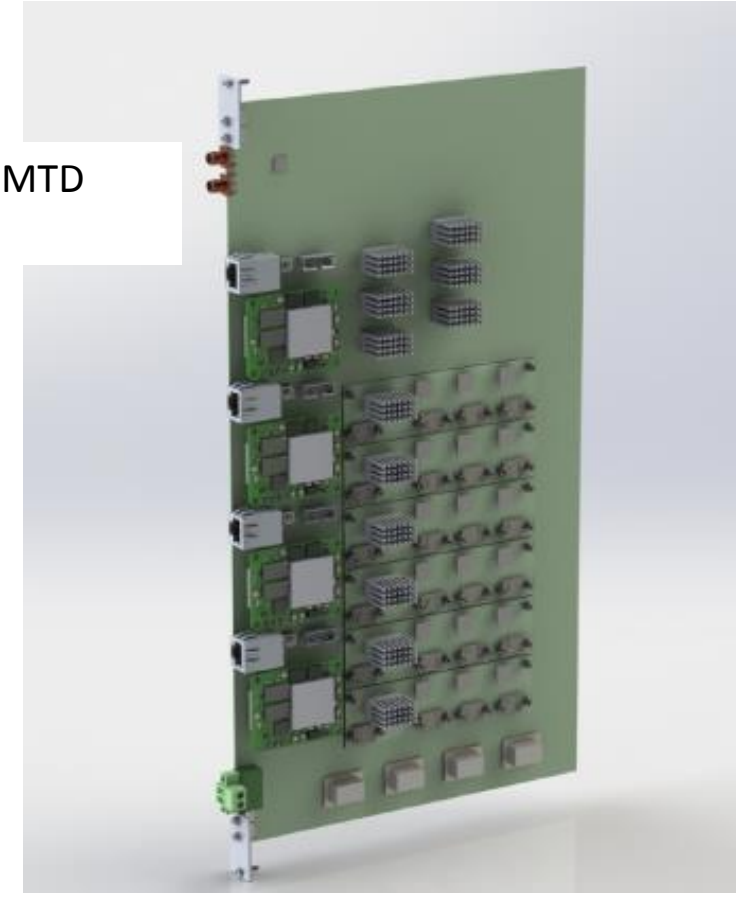
Next Step PCDM Demonstrator

Joint Saclay – Minnesota development to demonstrate distribution and monitoring of 72 channels of 160 MHz clocks.

Clock monitoring is done with 72 TDCs or 72 DDMTD circuits on 6 mezzanine boards.

In final details of circuit design. Layout to follow.





Summary

We have investigated methods for distributing a high precision clock and shown that a slave-to-slave time interval error (TIE_{SS}) of less than 1 ps is feasible.

We have developed the major components of clock distribution and phase monitoring system suitable for distribution to the ~10,000 channels of timing detectors that will be installed in CMS for the HL-LHC.

Acknowledgement

We are grateful to the hospitality shown to us by the CERN HPTD lab where many of the measurements reported here were made and one of us (RS) spent this summer making measurements and learning about clock distribution systems.

We are also grateful to the NSF, DOE and to CEA for their support in this project.

Backup

Instruments

- Microsemi 5125A

- Relative phase noise to a reference
- Offset frequency range: 1Hz to 1MHz

https://www.microsemi.com/product-_directory/phase-noise-and-allen-deviation-_testers/4129-5125a

---

Agilent E5052B

- Absolute phase noise
- Offset frequency range: 1 Hz to 40 MHz

https://www.keysight.com/en/pd-_1081579-pn-E5052B/ssa-signal-_source-analyzer-10-mhz-to-7-ghz-_265-ghz-or-110-ghz?cc=US&lc=eng

---

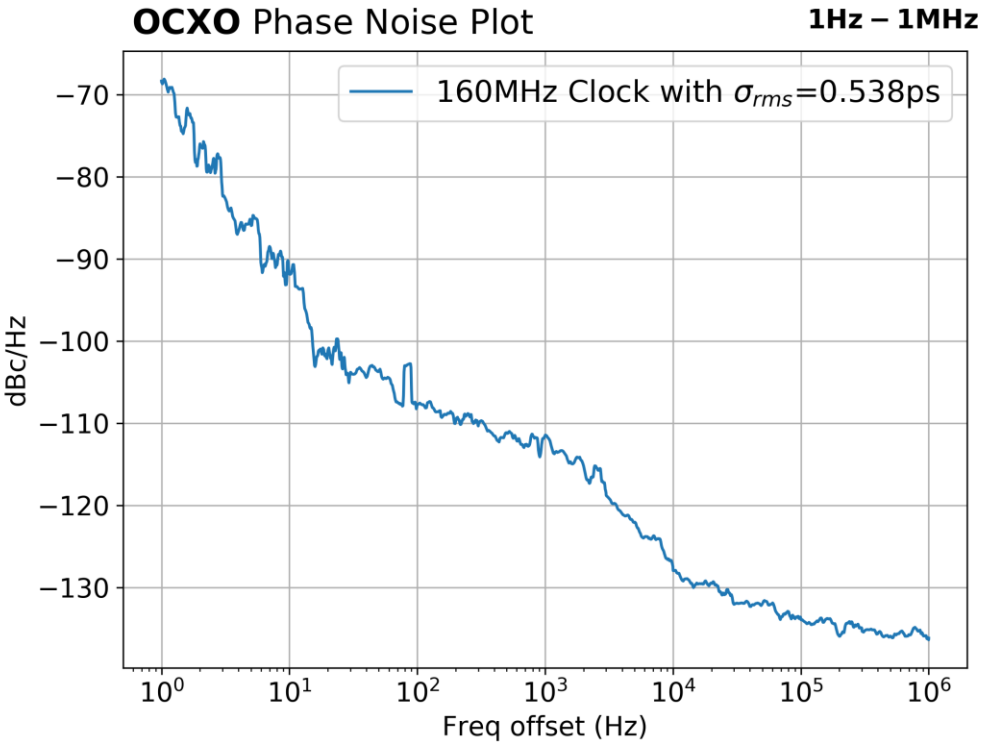
- LeCroy SDA 820Zi-B

- Clock skew → distribution → stdDev
- SDA analysis: σ, Random and Deterministic jitter.

http://teledynelecroy.com/oscilloscop_e/wavemaster-sda-dda-8-zi-b-_oscilloscopes/sda-820zi-b

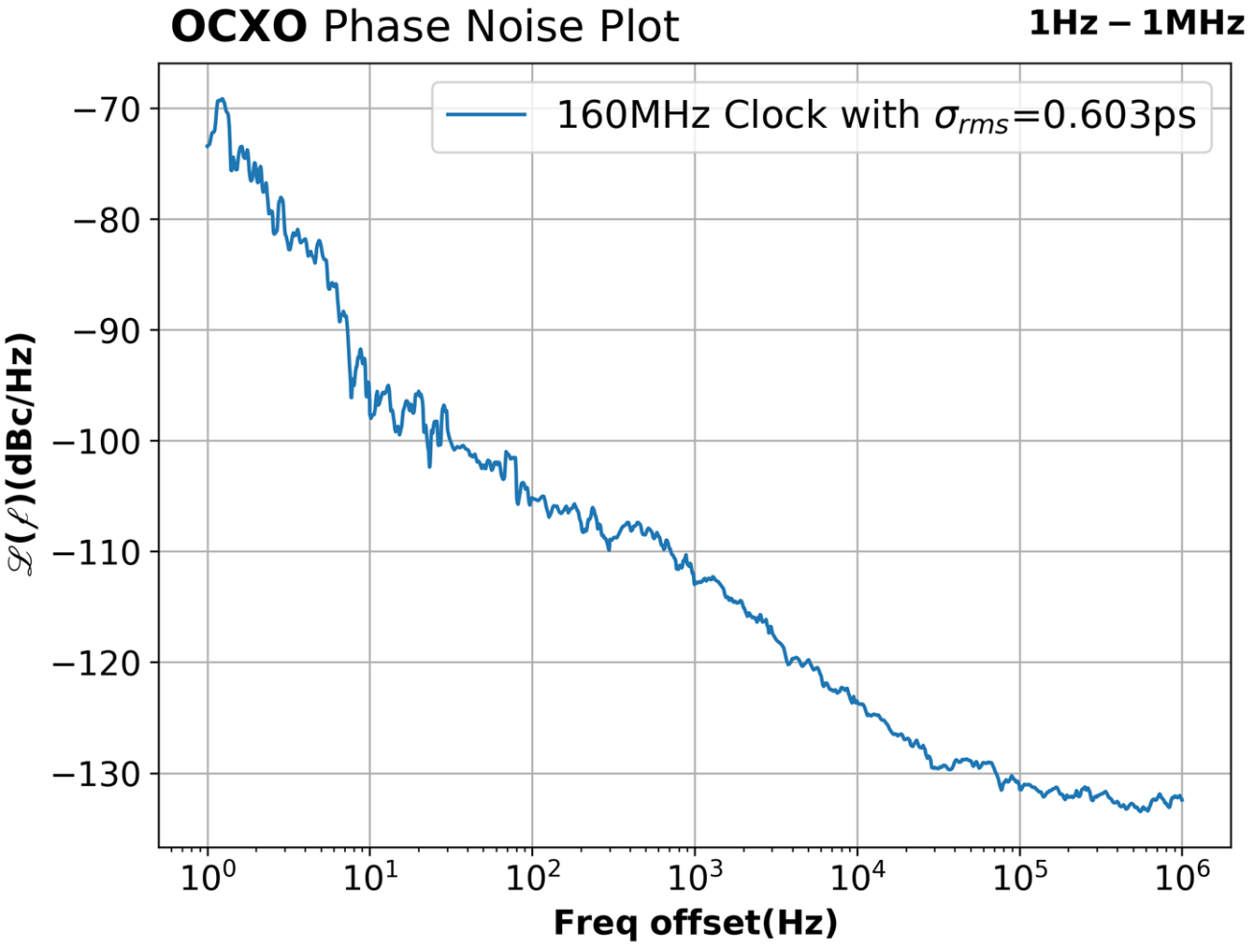
Using simple clock

Use an oven controlled crystal oscillator (OCXO) to produce a low-cost clock in Minnesota



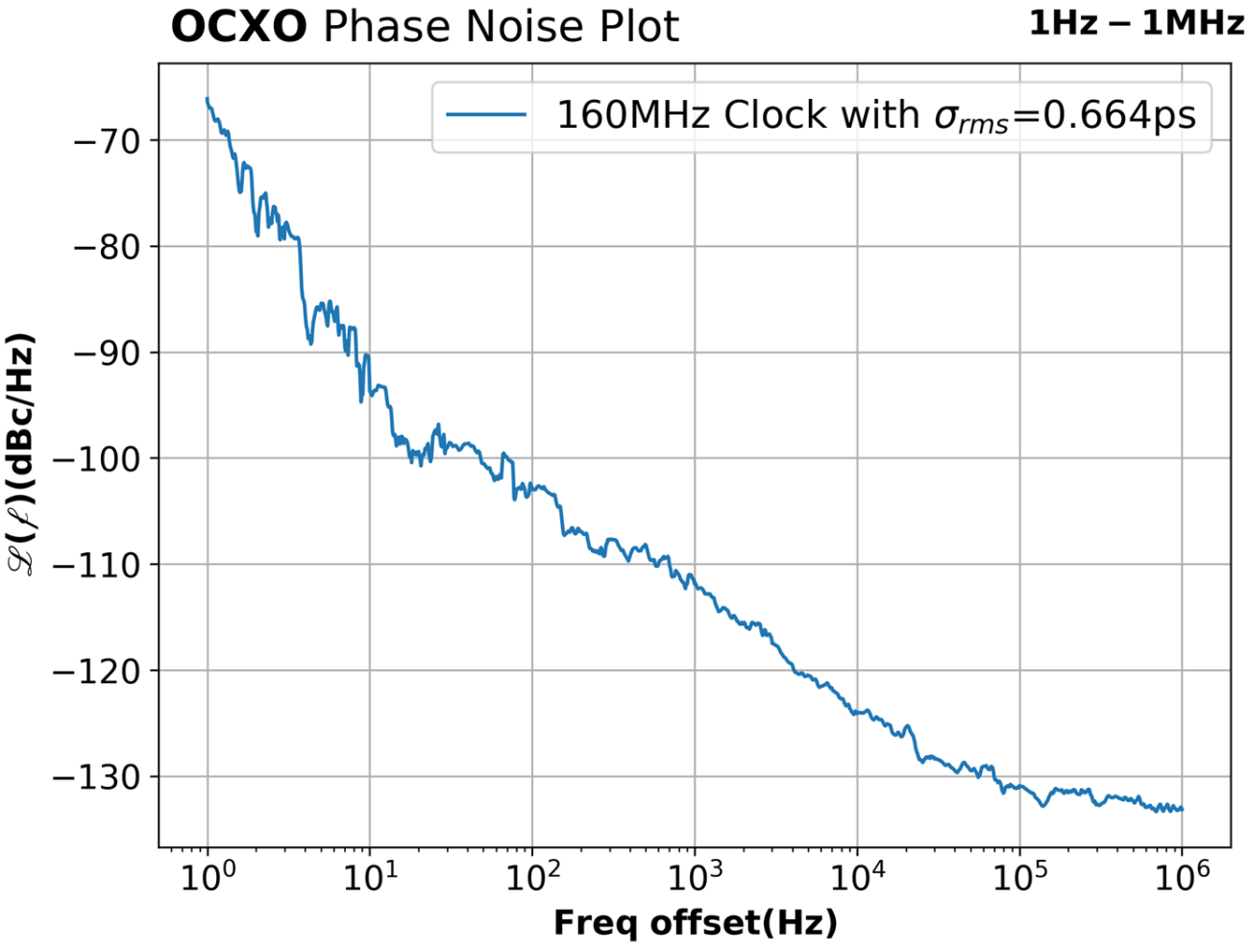
SFP - 1

90m Fiber



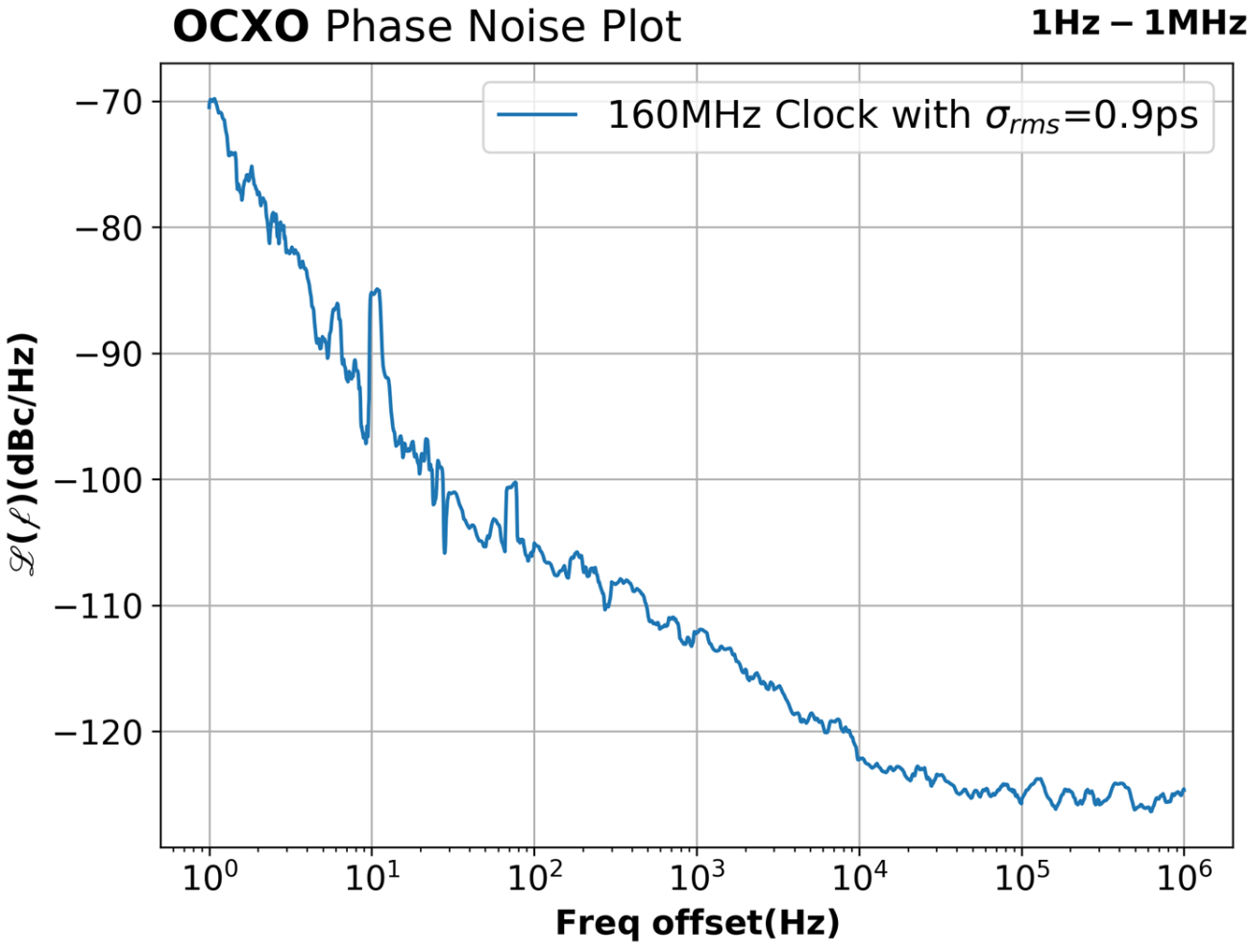
SFP - 2

90m Fiber



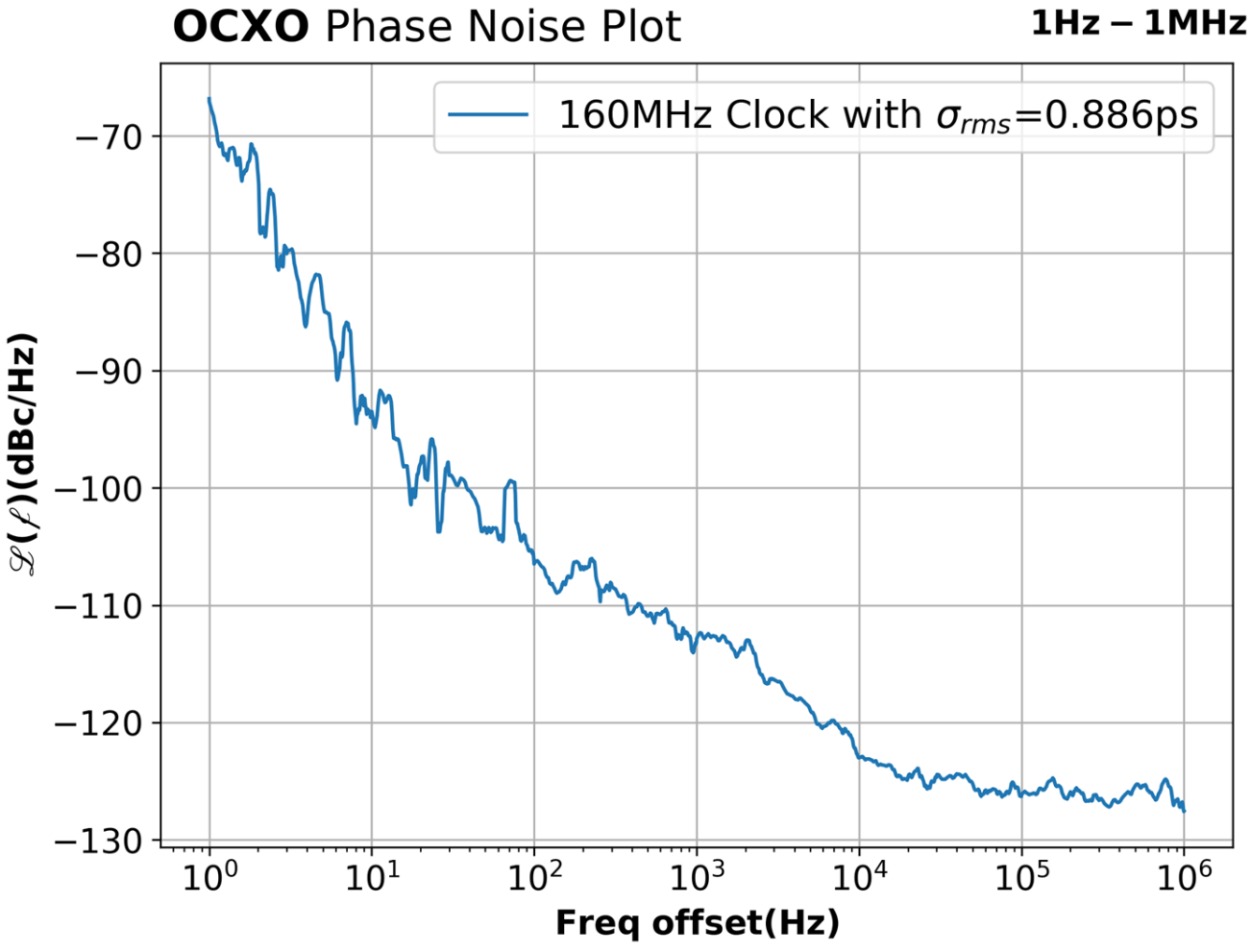
VTRx - 1

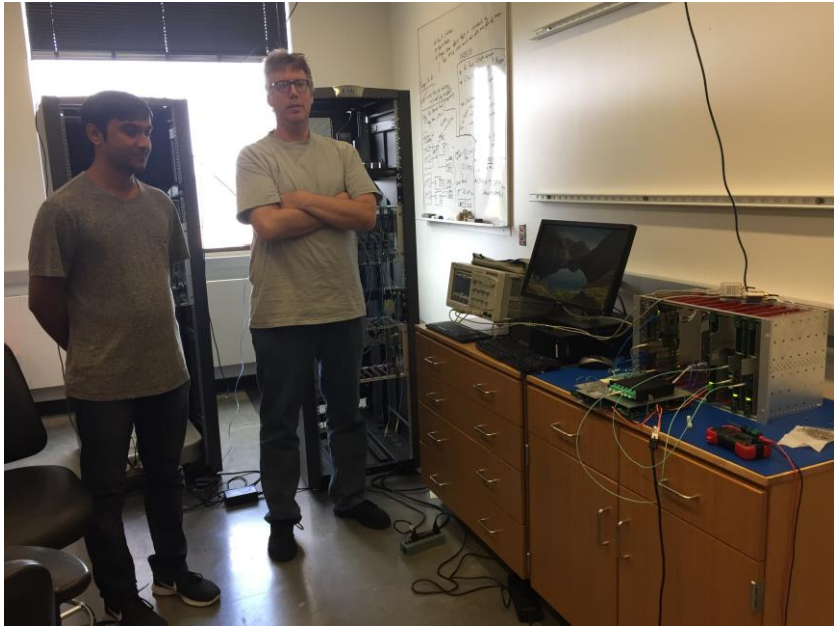
90m Fiber



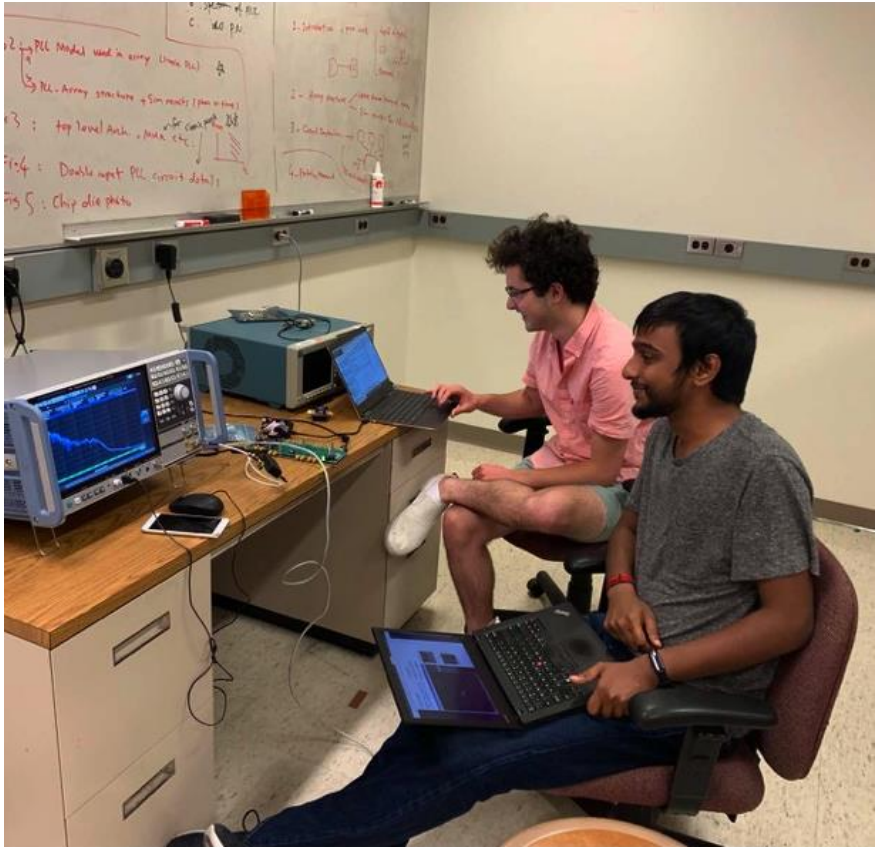
VTRx - 2

90m Fiber





Rohith Saradhy and Erich Frahm



Jonathon Brashear and Rohith

VTRx Test Setup