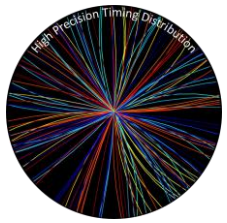


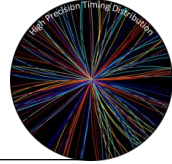
TCLink

A Timing Compensated High-Speed Optical Link for the HL-LHC experiments

Eduardo Mendes

On behalf of the HPTD team (E. Mendes, M. Taylor, S. Baron)

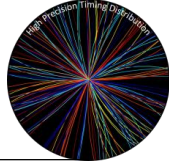
HPTD project



- High Precision Timing Distribution for HL-LHC

- Launched March 2018 (Aces 2018)
- Regular reports publication on SharePoint site
- Gitlab projects
- Active Community - Interest Group: HPTD-interest-group@cern.ch
- Regular meetings
  - Next one Sept 24 at CERN

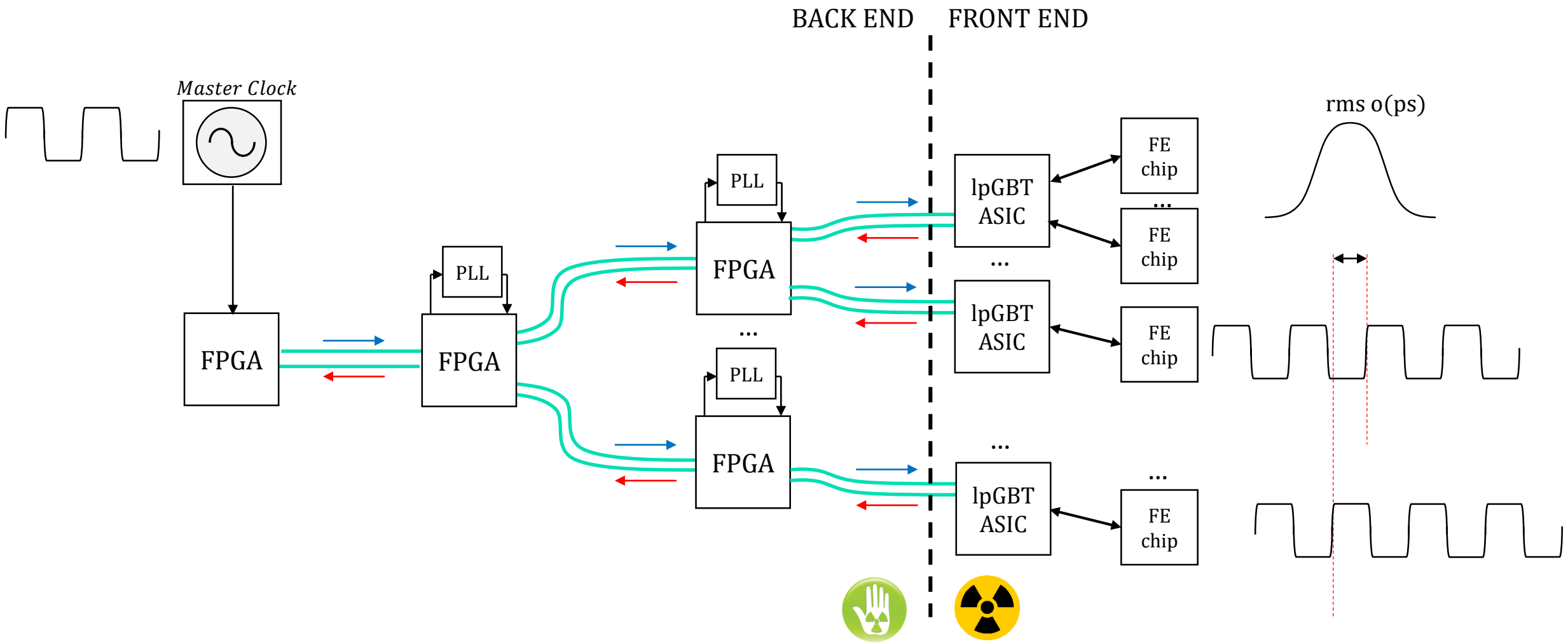
Outline



- Timing Distribution for HL-LHC
- Timing Compensated Link
- Experimental Results
  - Fiber Temperature Variation
  - Loop dynamics test
- Conclusion and Next Steps

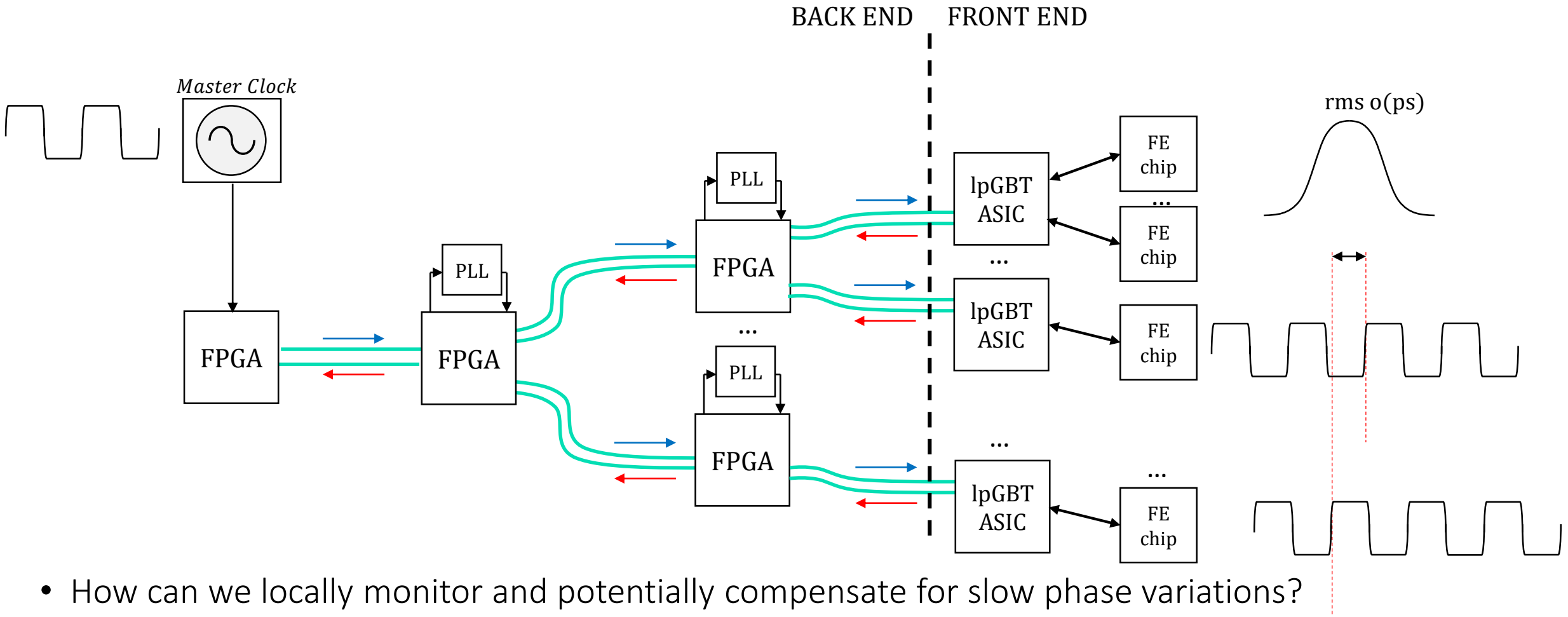
Timing Distribution for HL-LHC

- **Timing**, Trigger and Control based on high-speed serial links



Timing Distribution for HL-LHC

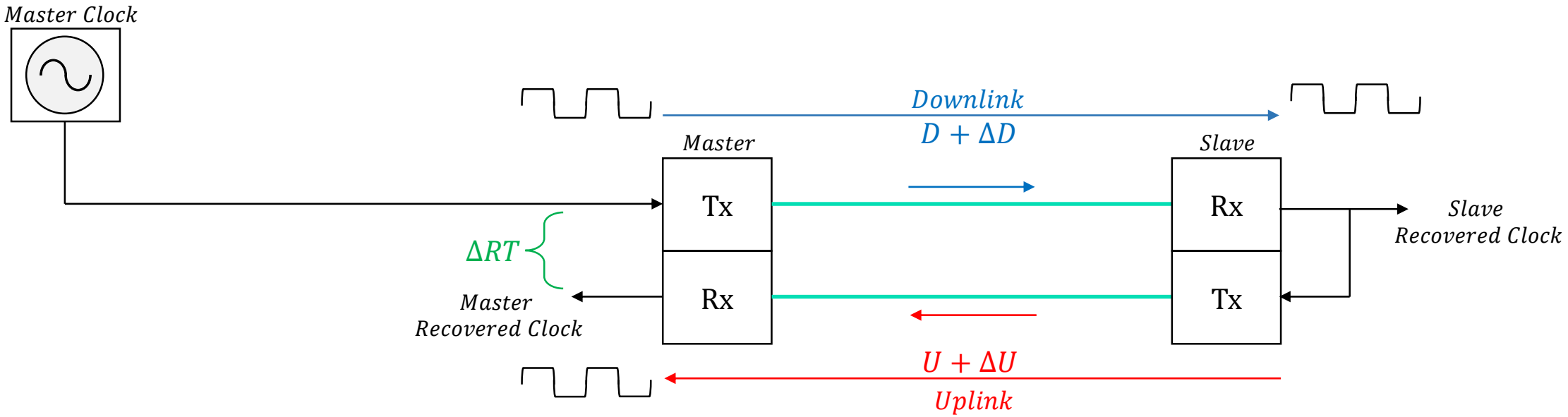
- Fast phase variations (<o(1ms)) are filtered by last back-end PLL of the chain
- Slow phase variations due to environmental changes impact phase of recovered clock



- How can we locally monitor and potentially compensate for slow phase variations?

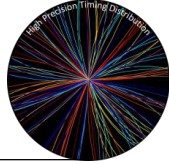
Timing Compensated Link - Principle

- Timing compensated optical links are not a brand new thing [1][2]…

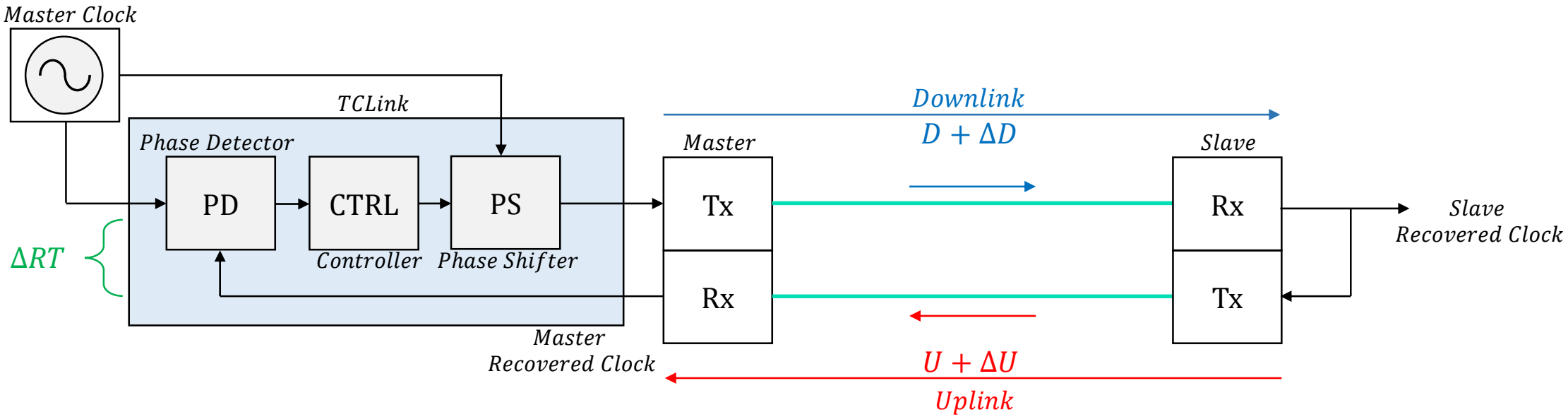


- Principle:
  - bidirectional synchronous link
  - Roundtrip phase **measurement** (ΔRT) and partial **compensation** (ex. $\Delta D = 0.5 * \Delta RT$)

Timing Compensated Link – Building blocks



- **Fully-integrated** in FPGA

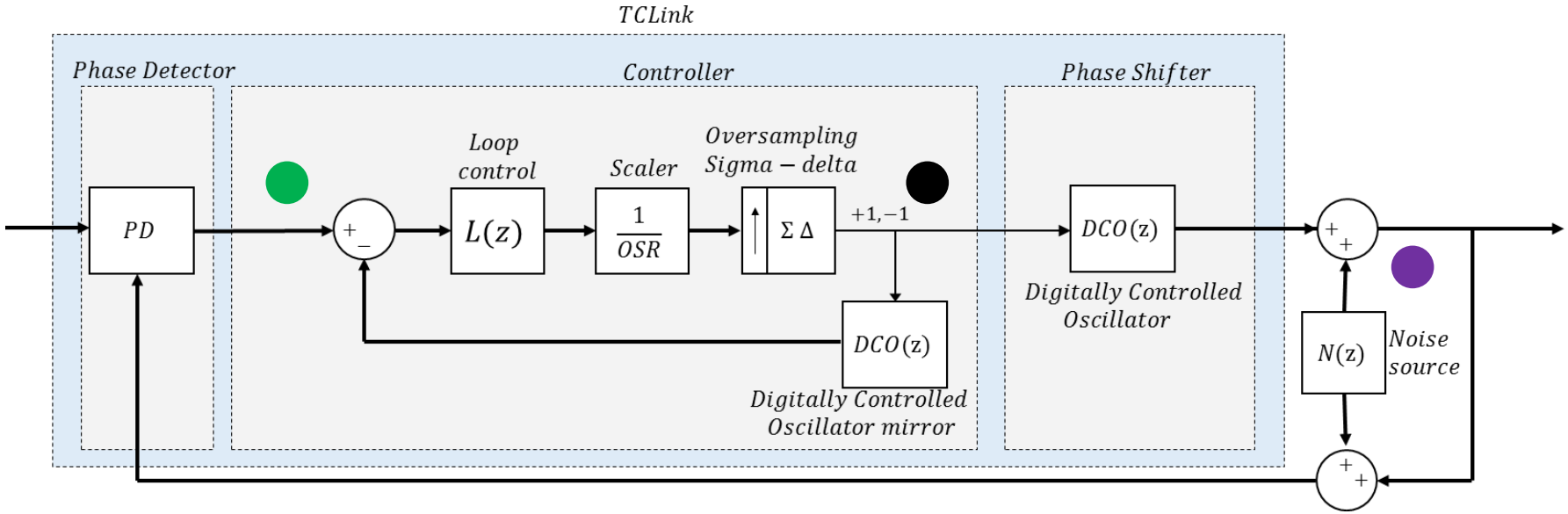


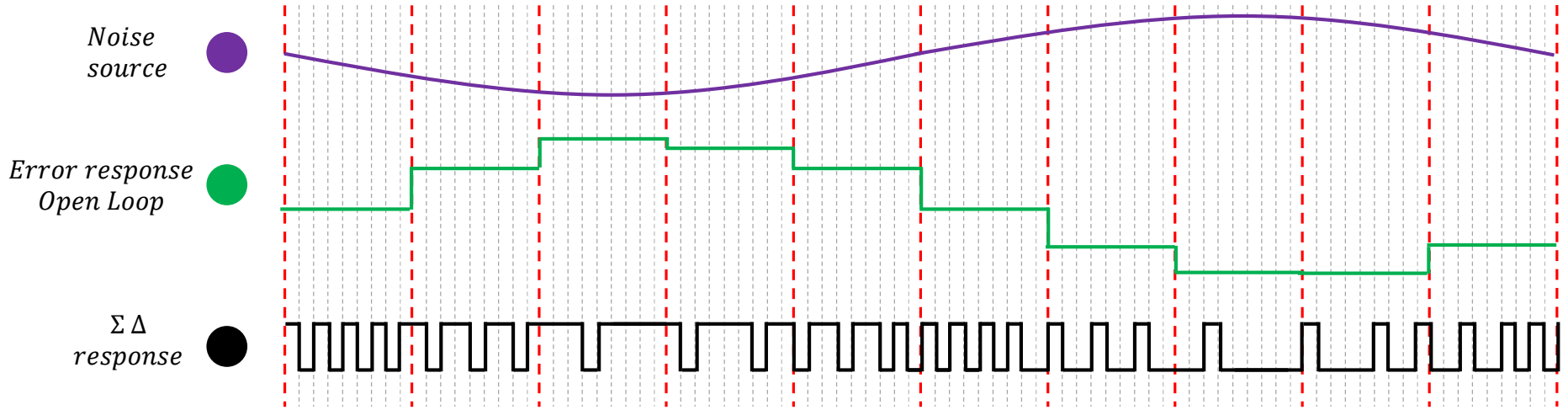
- **Phase-detector:** Digital dual mixer time difference (DDMTD) used in White-Rabbit [2][3]
- **Phase Shifter:** Xilinx FPGA transceiver Tx phase shifter (Tx phase interpolator) [4] using HPTD IP [5]
- **Controller:** custom digital core using All-Digital PLL techniques [6][7]

- **Design-flow**: high-level model (Matlab) → digital design and verification → hardware tests

Timing Compensated Link – Control diagram

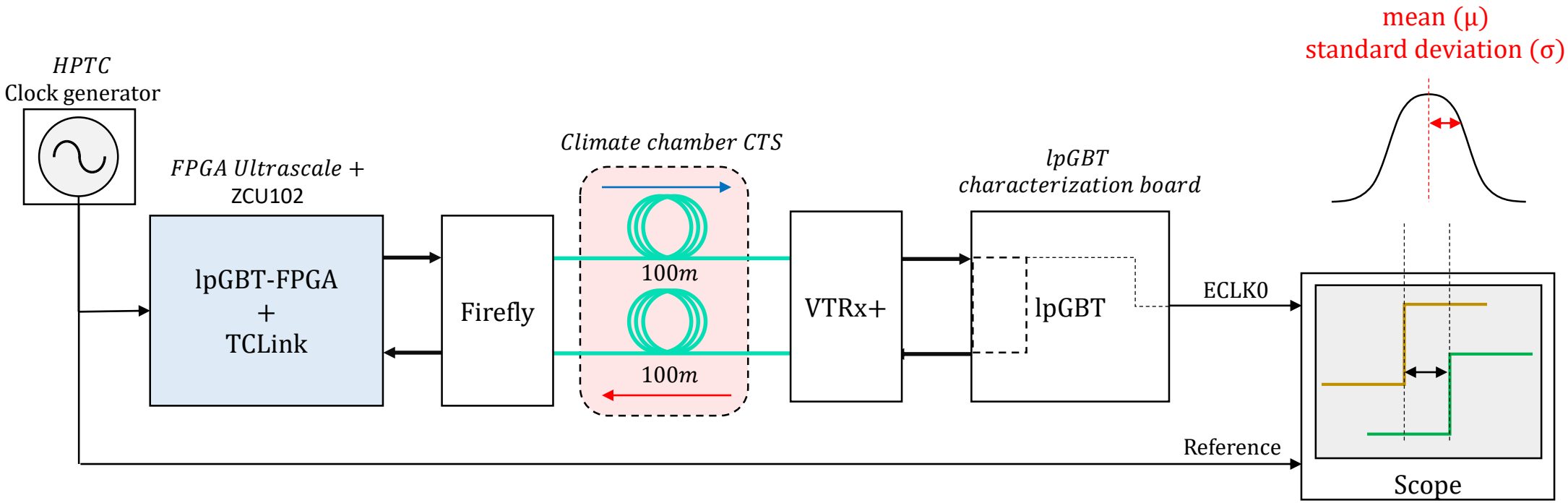
- Brief overview on controller diagram





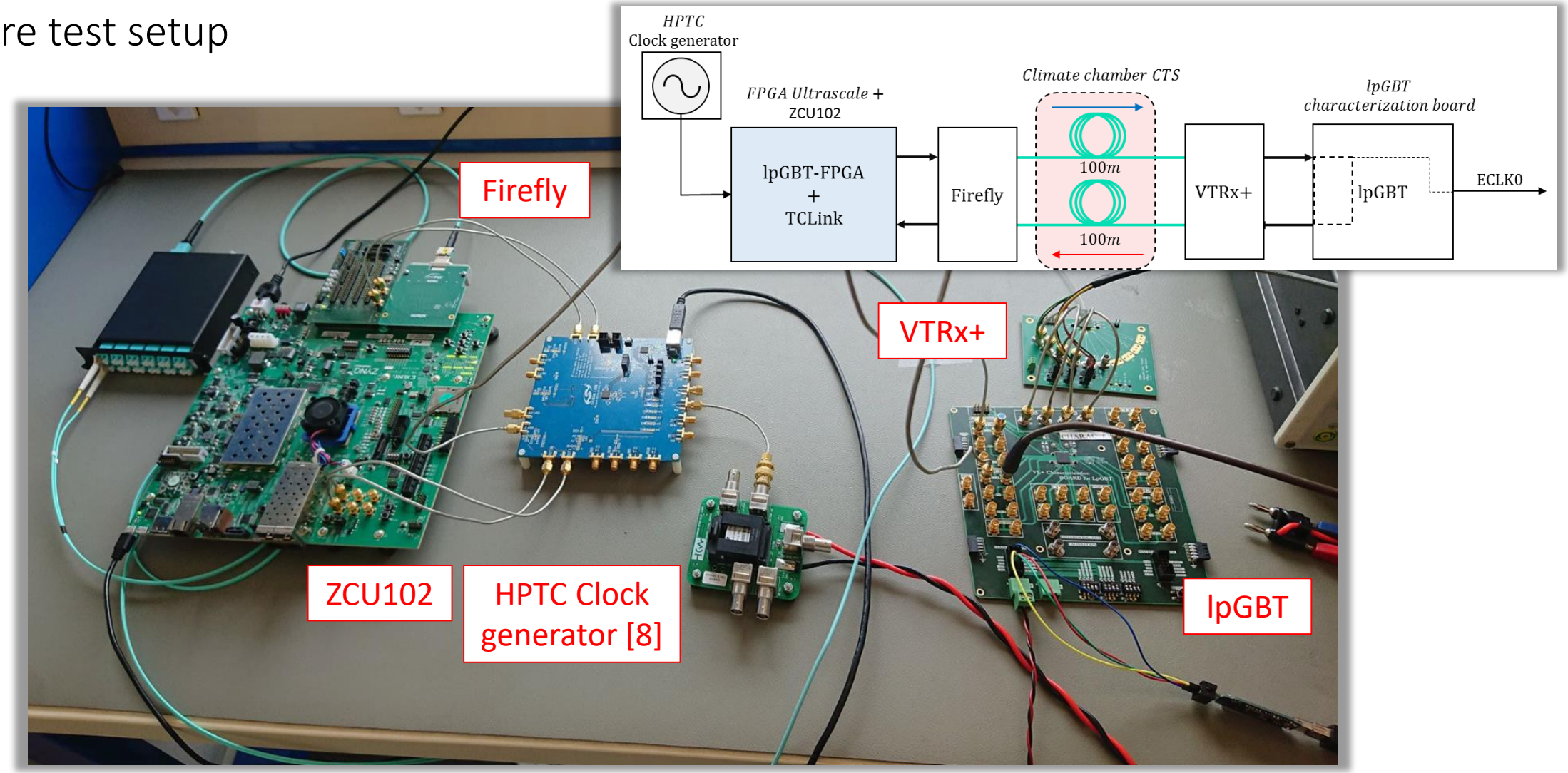
Experimental Results: Fiber Temperature Variation

- Fiber temperature variation test setup



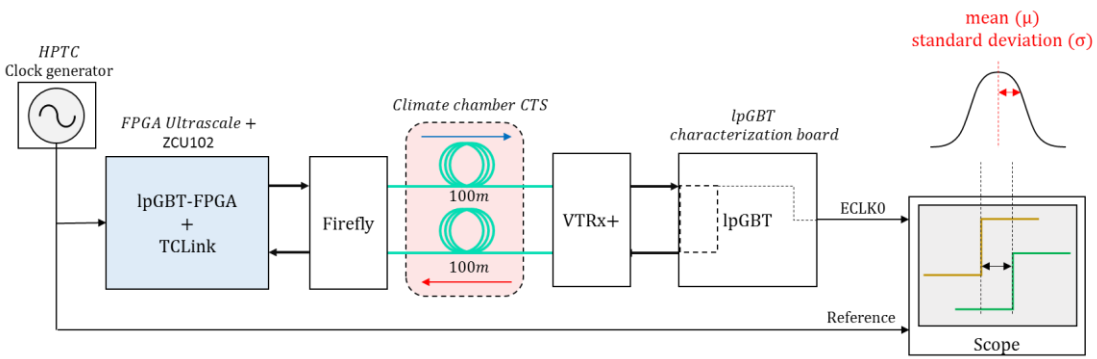
Experimental Results: Fiber Temperature Variation

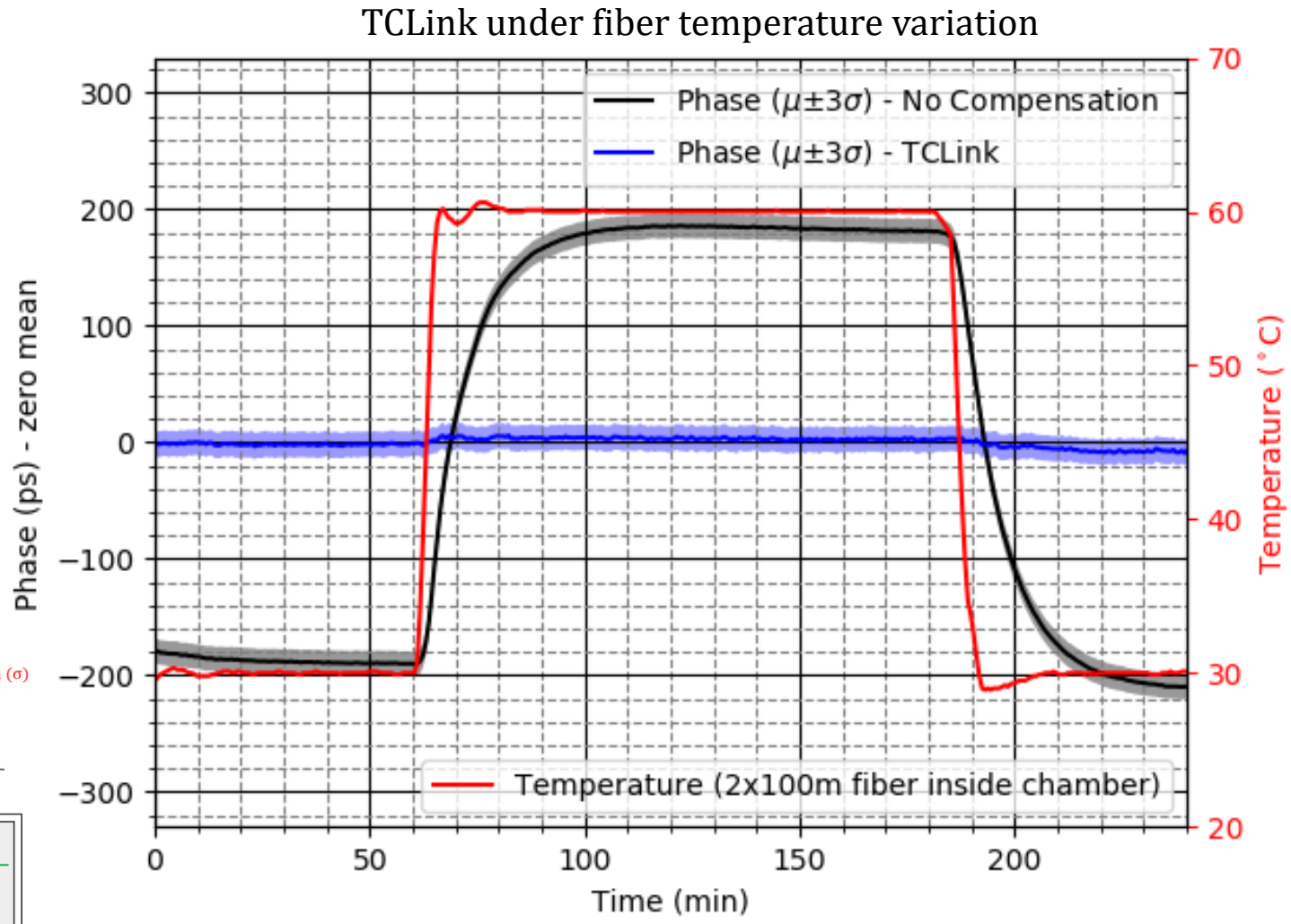
- Hardware test setup



Experimental Results: Fiber Temperature Variation

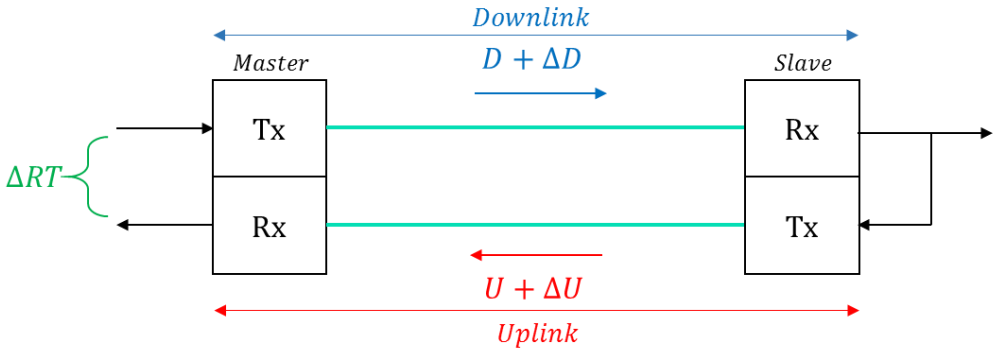
- TCLink loop controller tracks well phase variations due to fiber temperature drift
  - sub-ps correction capability
- Around 80x improvement compared to no compensated link

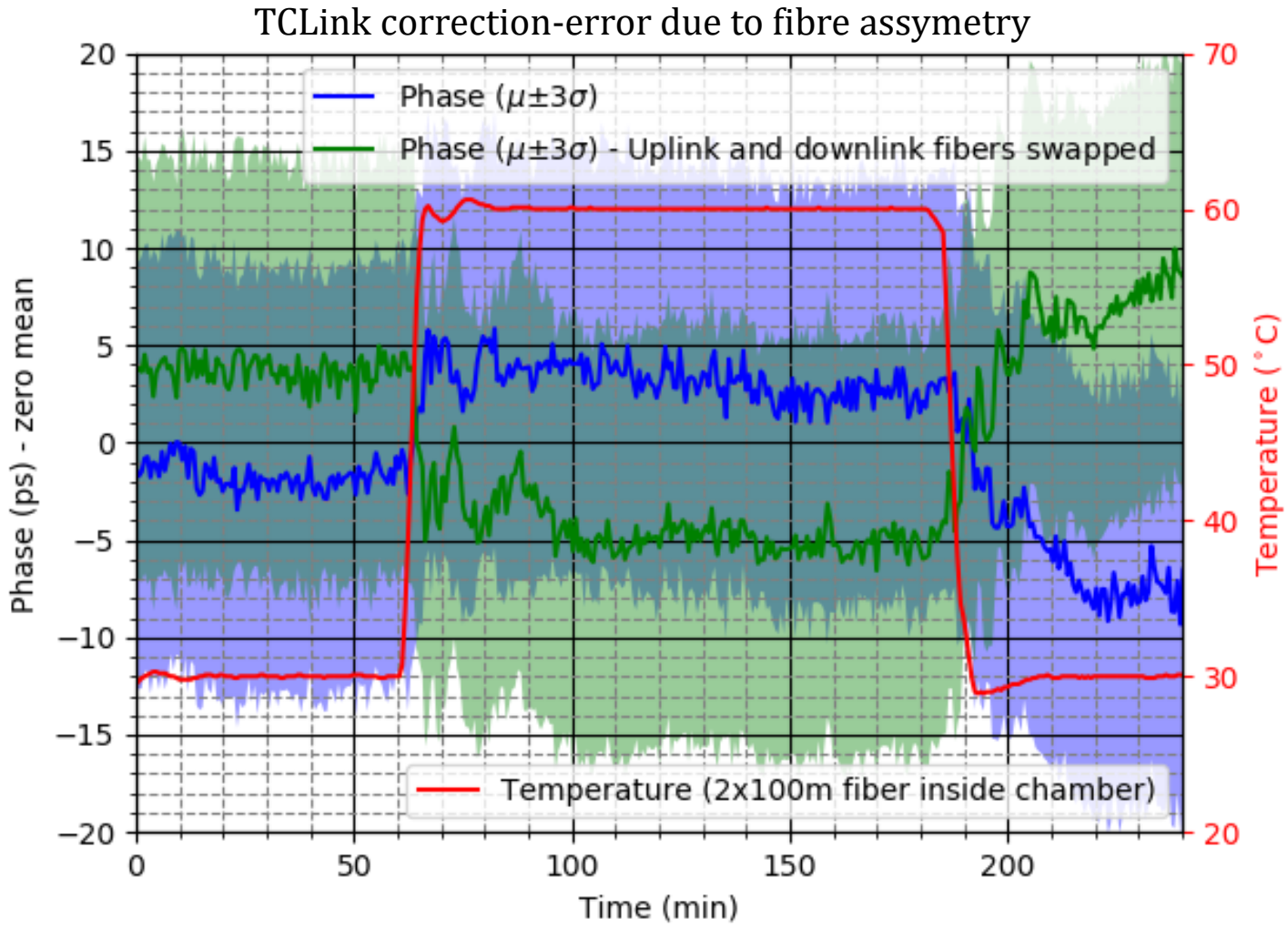




Experimental Results: Fiber Temperature Variation

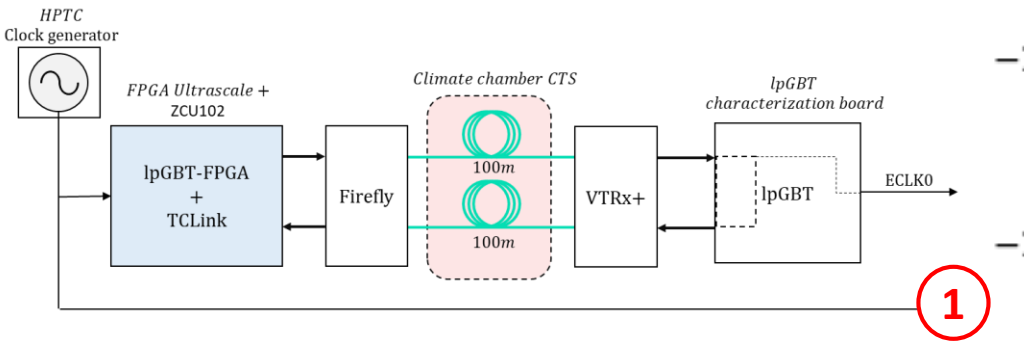
- Smooth operation
  - No systematic slow phase jumps are observed
- Remaining error related to symmetry hypothesis
  - $\Delta D = 0.5 * \Delta RT$
  - Swapping uplink and downlink fibers confirms this

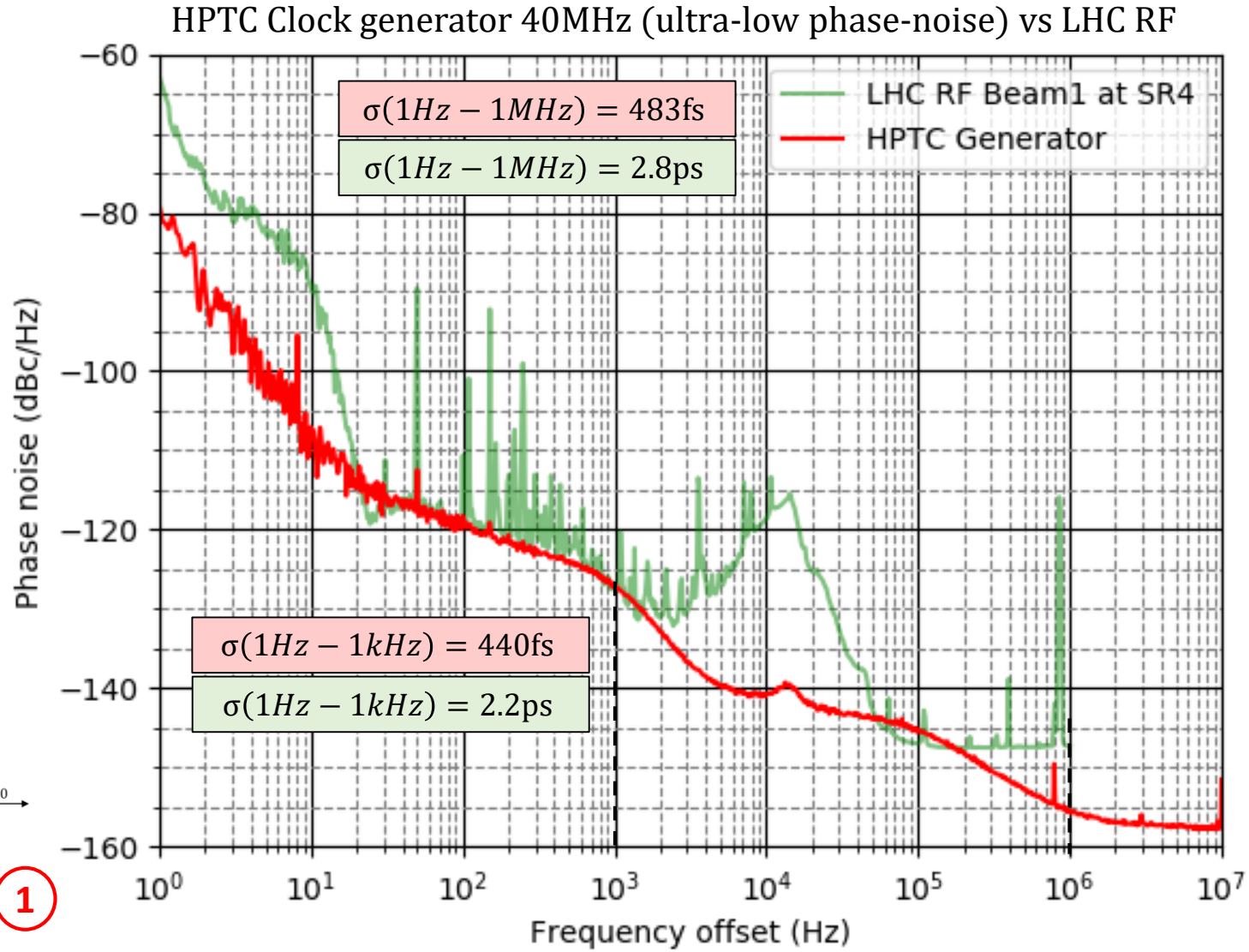




Experimental Results: Fiber Temperature Variation

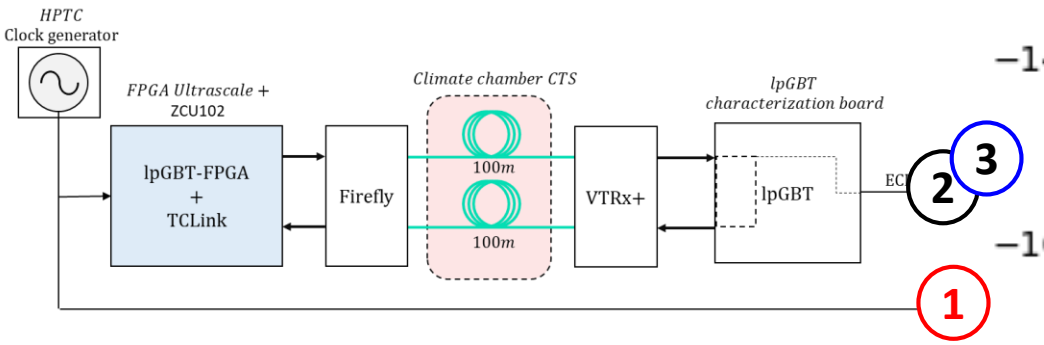
- Phase-noise basics
  - Frequency-domain analysis
  - Integral gives an rms jitter value
  - Measurements performed with phase-noise analyzer FSWP8

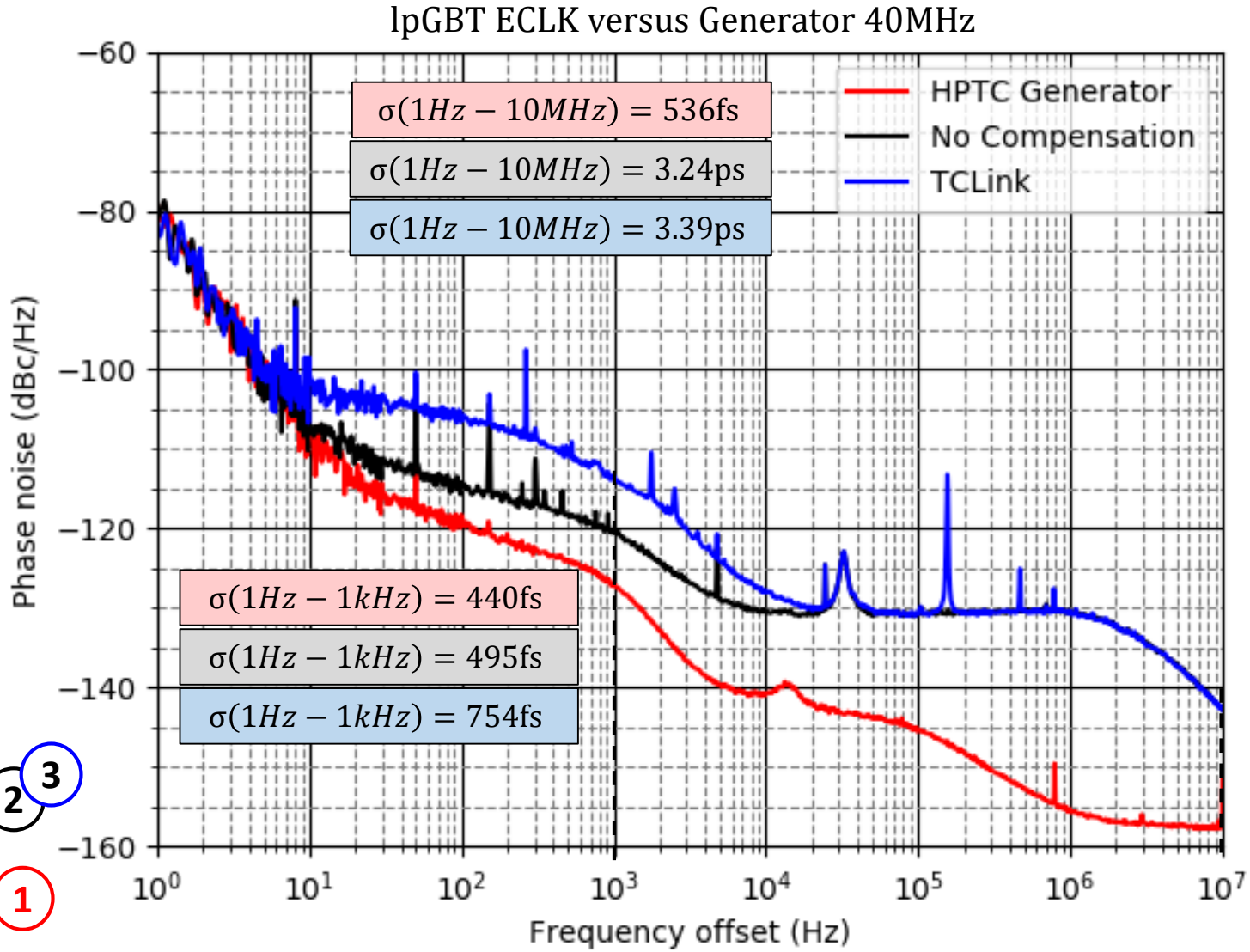




Experimental Results: Fiber Temperature Variation

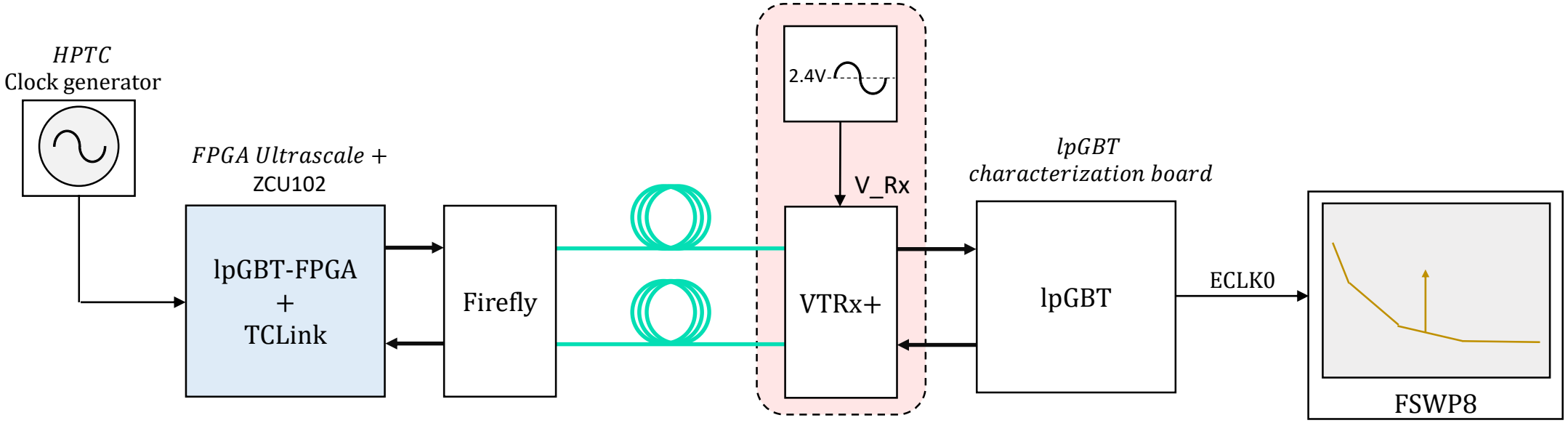
- TCLink penalty on phase-noise?
  - No major impact on clock quality
    - ~997fs rms within 1Hz-10MHz
    - ~569fs rms within 1Hz-1kHz
  - Despite excellent behaviour, still some room for improvement on controller parameters optimization





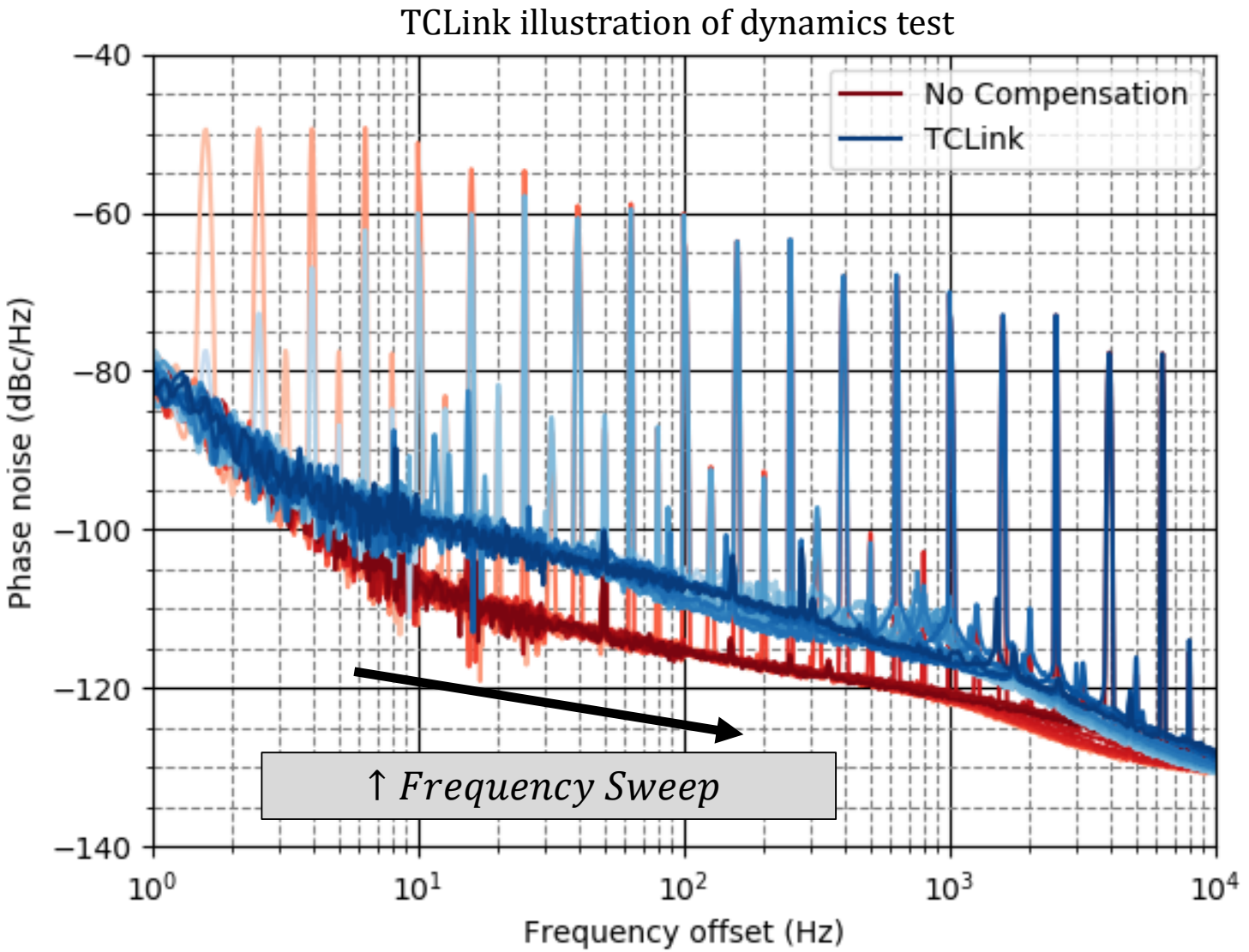
Experimental Results: Loop dynamics test

- Loop dynamics test
  - Modulating voltage with a small sinusoidal ripple → up-converted to phase-noise



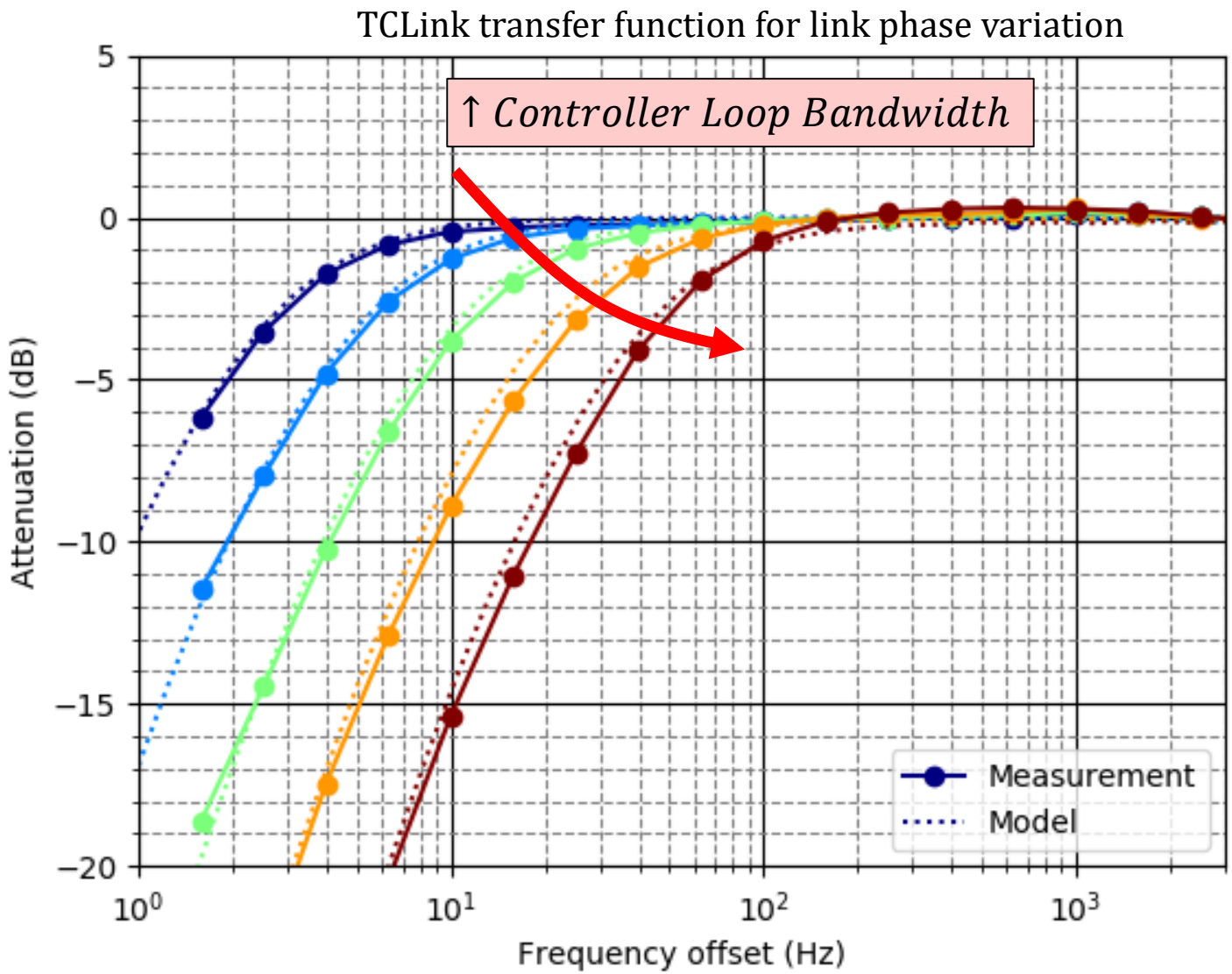
Experimental Results: Loop dynamics test

- Principle
  - Sweep in frequency for no compensation (open-loop) and TCLink (closed-loop)
  - Calculate transfer function at each frequency sweep point

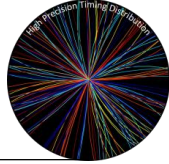


Experimental Results: Loop dynamics test

- Flexibility on user-choice of controller parameters
- Good agreement between measurements and model
- Be careful with bandwidth choice
  - It shall make sense w.r.t. environmental variations speed
  - Jitter increase
  - It has to be much slower than internal loops

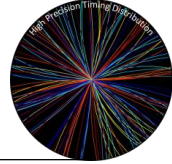


Conclusion



- The TCLink proof-of-concept is really promising
  - Tracks smoothly slow phase drift with a **sub-ps resolution** (accuracy depends on roundtrip hypothesis)
  - **No external hardware required and very little FPGA logic**
  - **Independent compensation** for multiple links in a single FPGA
  - **Can be implemented on any P2P serial link**
    - FPGA to FPGA, FPGA to lpGBT
    - Protocol agnostic
    - Compatible with TTC-PON fine phase monitoring feature for cascaded systems
  - At the cost of…
    - **Less than 1ps rms additive jitter**
    - Xilinx based

Next Steps

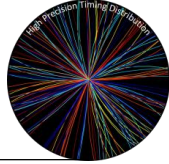


- More studies to come:
  - Impact of FPGA utilization and temperature on TCLink performance
  - Full-chain implementation (cascaded system) and characterization under realistic experiment conditions
  - Example design and application note to distribute to interested users (Gitlab)

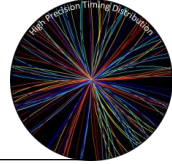
- Coming soon:
  - A more detailed presentation on this topics during upcoming HPTD interest group meeting (24/09/2019)
  - For more info, subscribe for our high precision timing distribution interest group

HPTD-interest-group@cern.ch

References



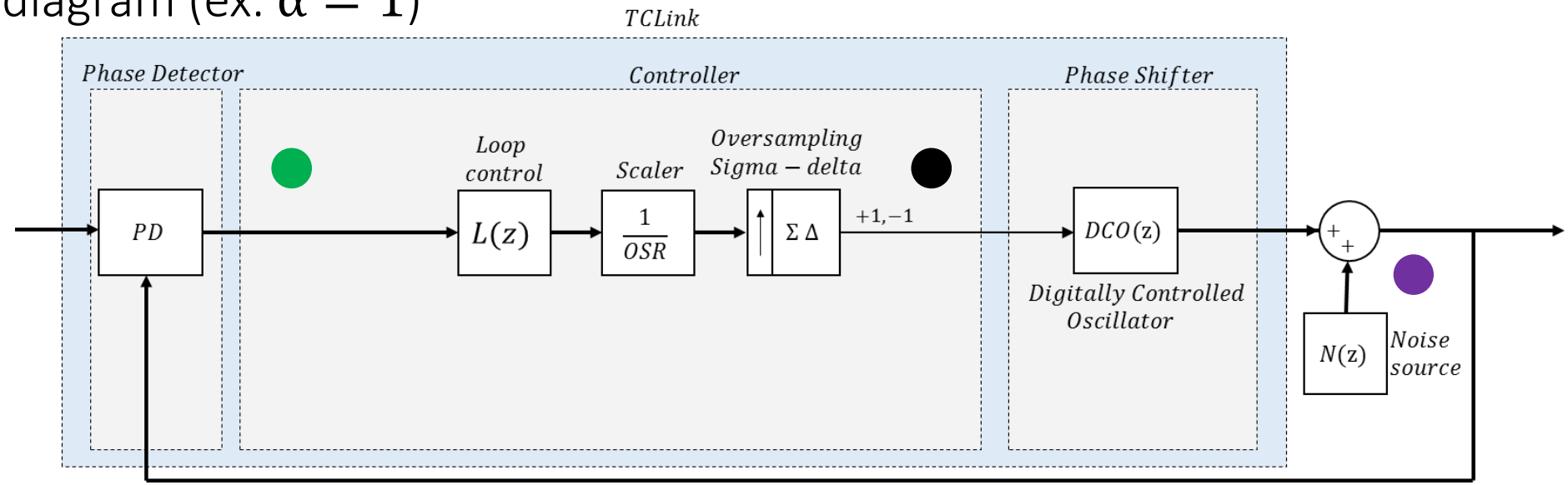
- [1] M. Calhoun, et al. «Stable photonic links for frequency and time transfer in the deep-space network and antenna array» in Proc. IEEE vol.95, pp.1931-1946, 2007
- [2] M. Rizzi, et al. «White-Rabbit clock characteristics» in Proc. IEEE Int. Symp. Precision Clock Synchronization Meas. Control Commun.., pp. 1-6, 2016
- [3] Open-hardware White-Rabbit project. Available online: https://www.ohwr.org/projects/white-rabbit
- [4] Xilinx, Ultrascale Architecture GTH Transceivers, UG576 Xilinx, 2018
- [5] E. Mendes, S. Baron, HPTD IP Core, 2018
- [6] F. M. Gardner, Phaselock Techniques, WILEY Third Edition, 2005
- [7] R. B. Staszewski, All-Digital Frequency Synthesizer in Deep-Submicron CMOS, WILEY, 2006
- [8] M. Taylor, E. Mendes, Short-term clock quality of Silicon Labs PLL (Si5344) with OCXO, 2019

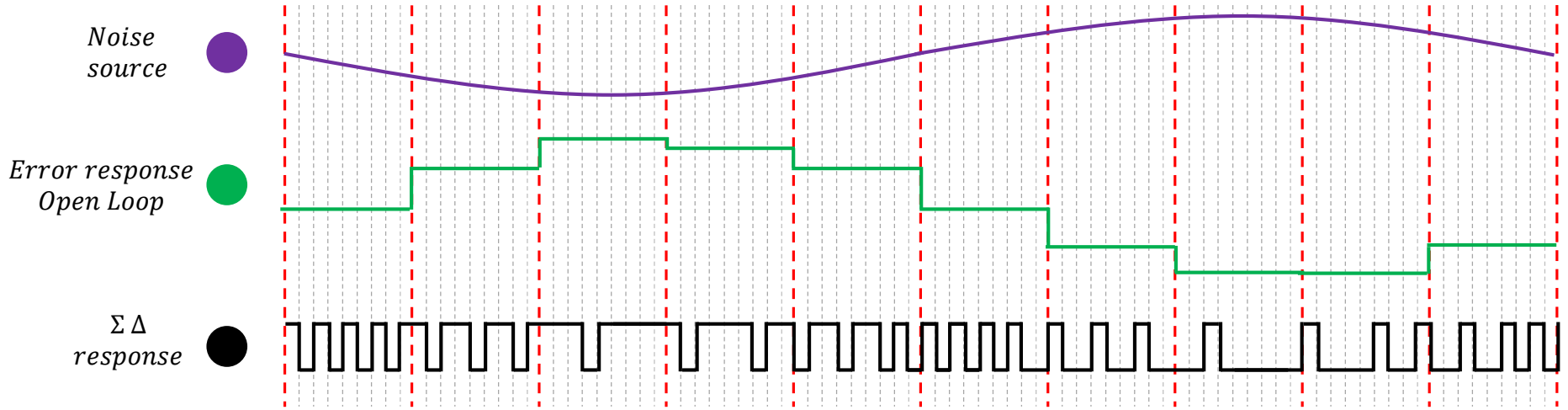


SPARE SLIDES

Timing Compensated Link – Control diagram

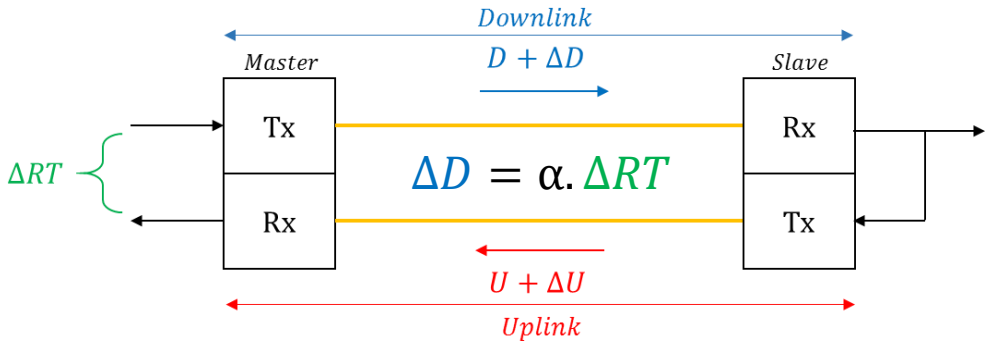
- Controller diagram (ex. $\alpha = 1$)

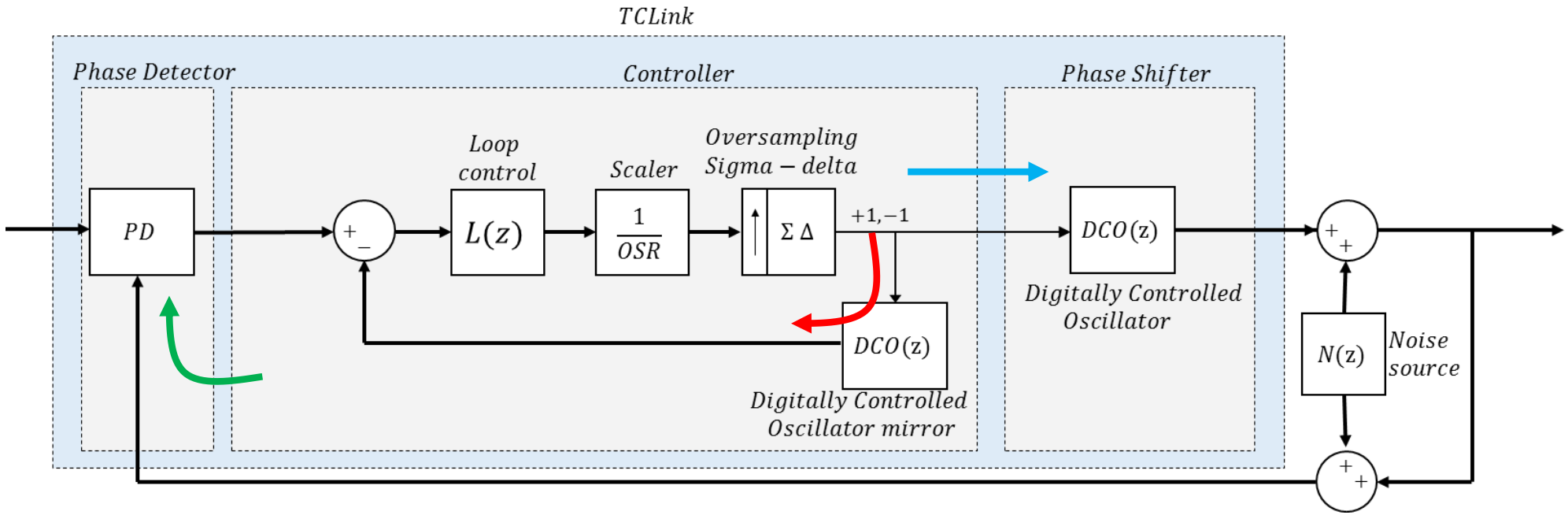




Timing Compensated Link – Control diagram

- Modified controller diagram for partial compensation
  - Internal mirror of the control plant
  - Example for $\alpha=0.5$

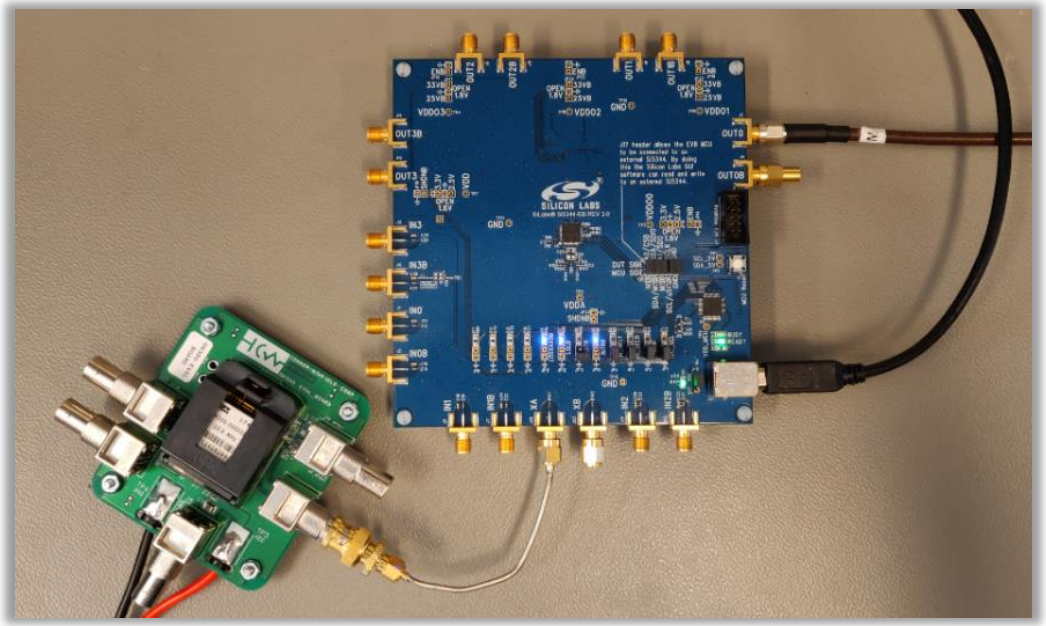




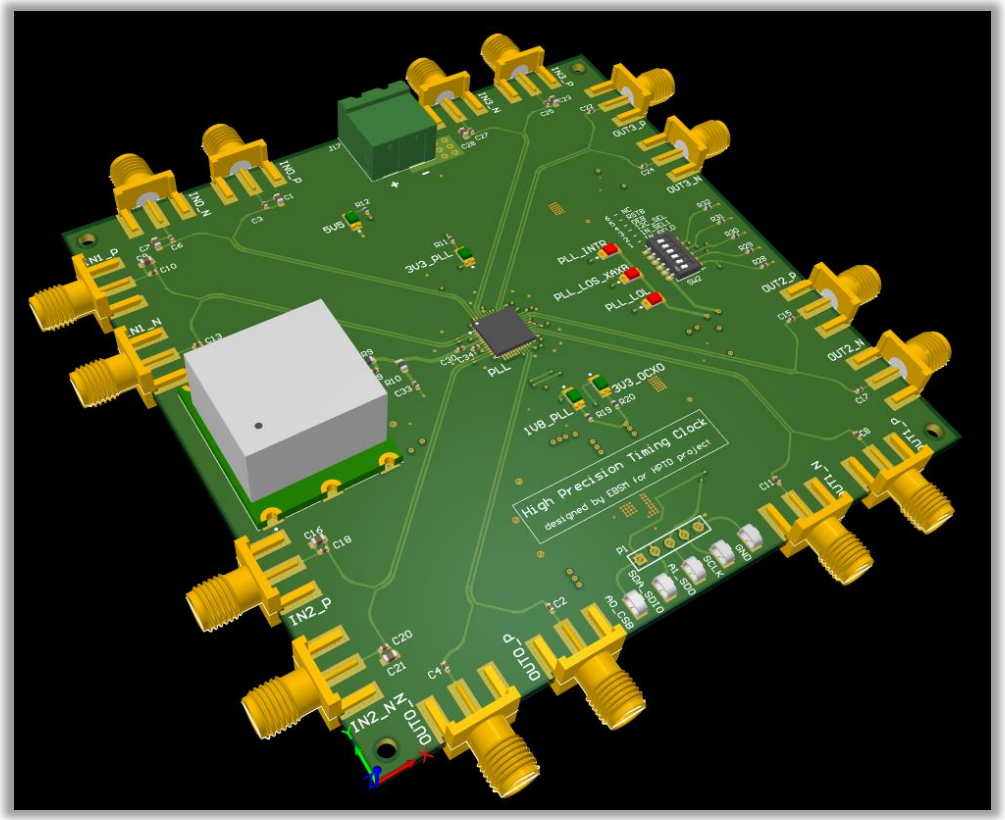
  - For other values of α, scale mirror path has to be scaled

HPTC Clock Generator

- Connor Winfield SC-cut OCXO + Silicon Labs PLL
- Report on prototype1 (eval. boards): [report prototype1 HPTC]
- Prototype2 will be soon manufactured



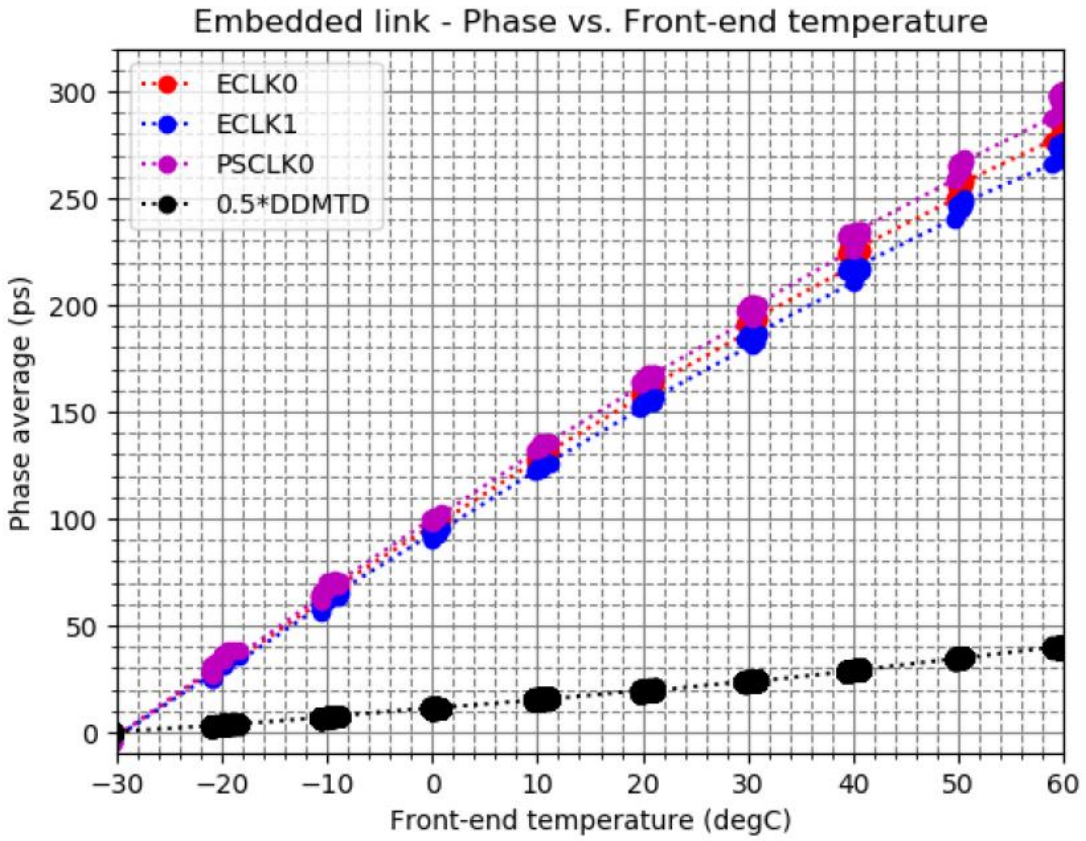
prototype1

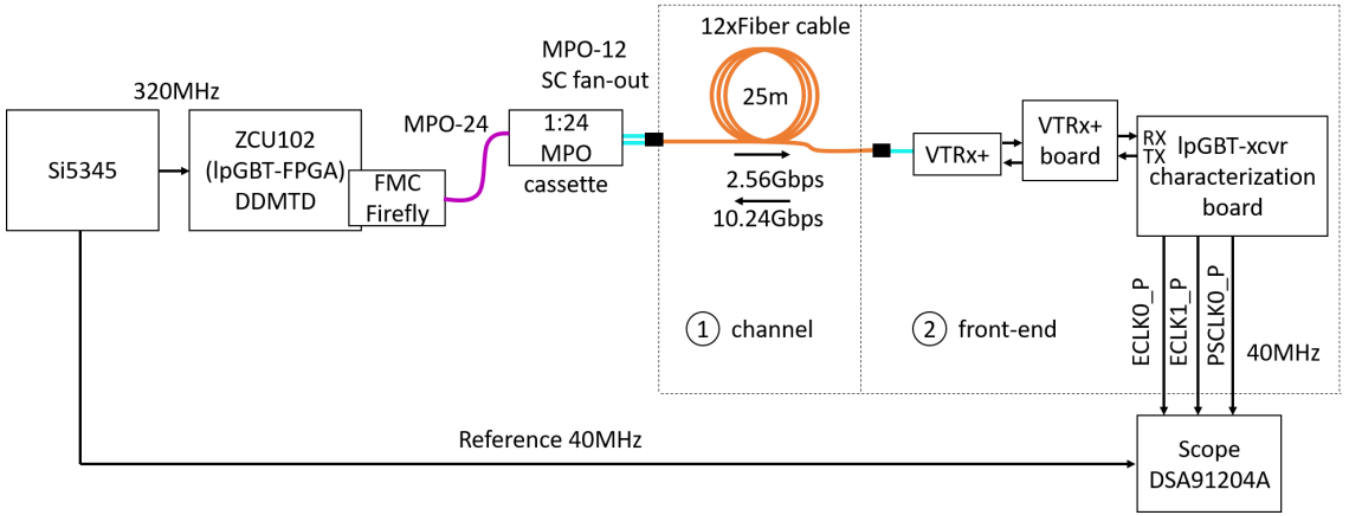


prototype2

Timing Compensated Link – lpGBT temperature

- Tests performed during timing-week with CMS colleagues in open-loop
  - lpGBT XCVR mode phase vs. temperature
  - Most of logic cannot be compensated





Timing Compensated Link – lpGBT temperature

- Tests performed during timing-week with CMS colleagues in open-loop
  - lpGBT XCVR mode feeding lpGBT TX mode phase vs. temperature