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TCLink: A Timing Compensated High-Speed Optical Link for the HL-LHC experiments

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The High-Luminosity Large Hadron Collider (HL-LHC) will pose unprecedented requirements in terms of timing distribution. The overall stability has to reach picosecond-levels between tens of thousands of end-points. To mitigate long-term environmental variations in the high-speed optical links, phase monitoring and online/offline compensation might be necessary. The Timing Compensated Link (TCLink) is a protocol-agnostic FPGA core that provides monitoring and picosecond-level phase adjustment capabilities. The features can be customized for different user application requirements. A proof-of-concept of TCLink on a setup composed by a Xilinx FPGA evaluation board, the Versatile Link+ and the lpGBT test chip will be demonstrated.

Summary

In order to cope with the high-levels of pile-up expected in the High-Luminosity Large Hadron Collider (HL-LHC), the CMS and ATLAS experiments will use timing information to distinguish between different collisions. This poses challenging requirements in the timing distribution network not to jeopardize the performance of the high-resolution timing detectors which will be installed in the experiments. The stability of the timing distribution network has therefore to reach picosecond-levels.

The baseline timing distribution in the HL-LHC experiments consists of thousands of high-speed optical links responsible for delivering the Timing, Trigger and Control (TTC) information. The back-end part (where no radiation is present) of the timing distribution network is usually represented by FPGAs having multiple transceivers coping with Gbps data-rates. Their front-end counterpart is the radiation-hard low-power Gigabit Transceiver (lpGBT) ASIC, a key player to deliver the TTC signals to the front-end chips.

In 2018, CERN has launched the High-Precision Timing Distribution (HPTD) interest group to study the short- and long-term timing stability performance of different timing components present in the baseline scheme to ensure they can cope with the stringent timing requirements posed by HL-HLC. Studies on the short-term stability of a Versatile Link+ and lpGBT based high-speed optical link have shown that a sub 5-picosecond rms level can be reached. However, long-term stability performance was not yet discussed at that time.

Long-term stability due to environmental variations such as temperature might play a key-role in the overall timing distribution stability. The monitoring and online/offline compensation of the phase of the lpGBT clocks might be necessary in order to reach the picosecond-level requirements.

As part of the HPTD project, the Timing Compensated Link (TCLink) concept was developed. The TCLink is a protocol-agnostic FPGA core envisaged to mitigate long-term variations in high-speed optical links. The concept is to have monitoring and picosecond-level online adjustment capabilities which can be tailored by the user to best fit his/her own convenience and application requirements.

In this paper, a proof-of-concept of the TCLink based on a Xilinx Ultrascale+ FPGA evaluation board, the Versatile Link+ and the lpGBT test chip will be demonstrated. Temperature variations in the different parts of the system (FPGA, fiber and lpGBT) are emulated with a climate chamber and its effects are discussed.

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