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Design and operation of radiation hard 65 nm drivers for Silicon Photonics based optical links

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We will present the design and the performance of two drivers in 65 nm TSMC technology, for Silicon Photonics Mach-Zehnder Modulator (MZM) devices, able to withstand radiation levels of up few 1016 n/cm2 and ~0.5 - 1 Grad. The drivers use a CML architecture and are optimized for >500 Mrad and a target a bit rate between 5 to 10 Gbps. They have been tested up to 800 Mrad showing about 25% degradation in voltage. Results of irradiation with ions will been shown. Finally, the results of operations with MZM and Ring-Resonators will be given and discuss the photonic-electronic integration.

Summary

Silicon Photonics is currently being investigated as an alternative to directly modulated laser-based radiationhard optical links [1]: custom-designed Mach-Zehnder Modulators (MZM) withstand non-ionizing energy losses (NIEL) of up few 1016 n/cm2 using shallow etch optical waveguides and high doping concentrations in their p-n junctions. In order to exploit the high bandwidths offered by MZM based systems (few tens of Gbps) careful design of drivers is required.

The drivers presented are designed to operate the MZM in [1] and to sustain similar TID, thus about 0.5 - 1 Grad. To be able to study the integration of the driver with the MZM, one driver has an internal pull-up resistor of 50 Ohm to possibly match the impedence of an external load, while the second doesn't, thus requiring an external regulator.

A CML (Current Mode Logic) architecture, designed in TSMC 65 nm technology, has been used to mitigate effects due TID and operate at a target bit rate between 5 to 10 Gbps. The core-MOSFETs having thin gate oxide are less affected by TID effects but, on the other hand, can sustain only 1.2 V, which doesn't match the 2 Vpp required to drive the MZM. To face this issue a cascode architecture is adopted in the last stage, which shares the output signals wide swing on the two-cascode MOSFETs. The driver has a $220 \times 175 \ \mu\text{m2}$ layout area and 149 mW power consumption. The post-layout simulations show a sustainable data-rate up to 10 Gbps.

The drivers have been fabricated by IMEC and received in September 2018. A printed circuit board (PCB) was designed to test the chip, whose naked die was glued on the board and its I/O pads wire bonded. The first driver was measured to deliver a single ended signal amplitude of about 1.2 V for a bandwidth up to about 3.5 GHz. The second driver (with internal pull-up) generates a single ended signal amplitude 1.2 V and a bandwidth of about 3 GHz. The eye diagrams show an open eye up to 5 Gbps. We are studying the reasons for the discrepancy between the expected performance of the chip after post-layout simulations and the actual measurement, addressing a non-optimal design of the board and of the wire-bonded connections. Measurements using a probe station are currently ongoing to bypass wire bonding and PCB effects.

The chip has been exposed to X-ray up to 800 Mrad, showing a degradation of the output voltage of about 25-30% for a signal frequency of 1 GHz. Tests with heavy ions have been performed, and results of the cross-section versus LET will be shown.

Finally, the chip was used to drive the MZM and Ring-Resonator described in [1]. The results of the measurements show a 3 dB bandwidth of about 2 GHz. The eye diagrams for the MZM show an open eye up to 5 Gbps. **Authors:** CIARPI, Gabriele (Università di Pisa, INFN Sezione di Pisa); MAGAZZU, Guido (INFN Sezione di Pisa, Universita' e Scuola Normale Superiore, P); KRAXNER, Andrea (CERN); PALLA, Fabrizio (INFN Sezione di Pisa, Universita' e Scuola Normale Superiore, P); SAPONARA, Sergio (Università di Pisa); SCARCELLA, Carmelo (CERN); TROSKA, Jan (CERN); VASEY, Francois (CERN)

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