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Stabilization and Protection of the Shunt-LDO regulator for the HL-LHC pixel detector upgrades

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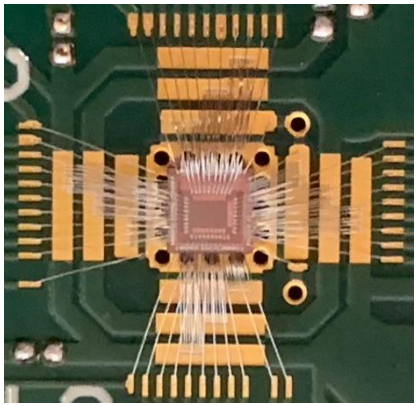
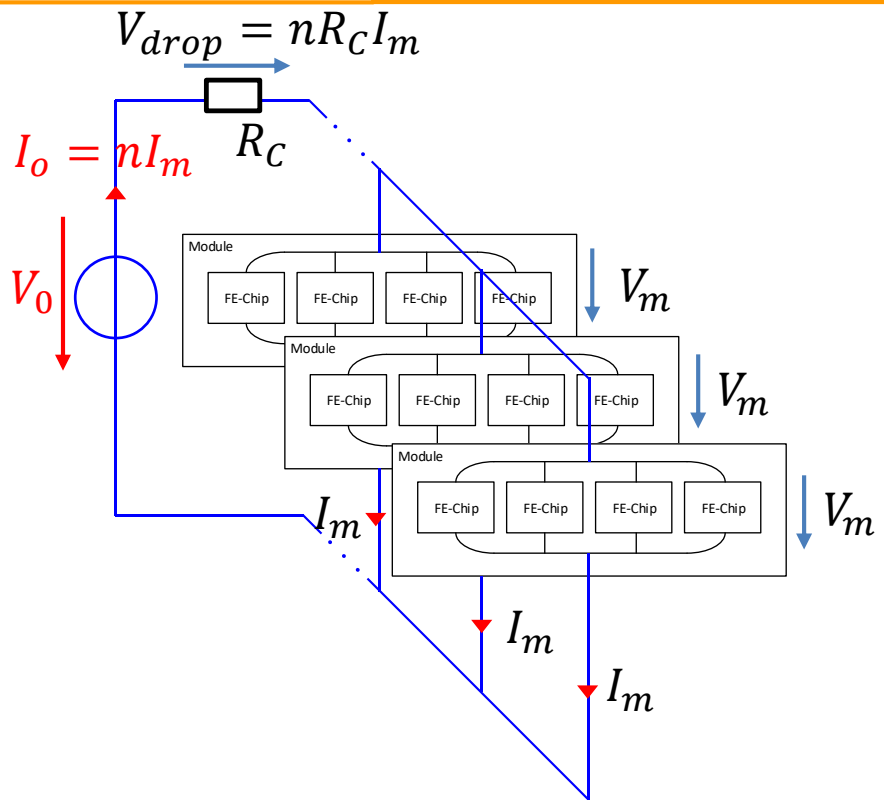
Introduction

- Serial powering is necessary for the supply of the pixel sensors in the Atlas and CMS experiment
- A voltage regulator is integrated in the front-end chips and generates a constant supply voltage from a constant supply current
- To stabilize the LDO regulator a new compensation scheme is introduced
- In order to generate precisely defined reference values for the regulator, the new revised Bandgap scheme is presented
- A number of new circuits have been added to ensure robustness and security

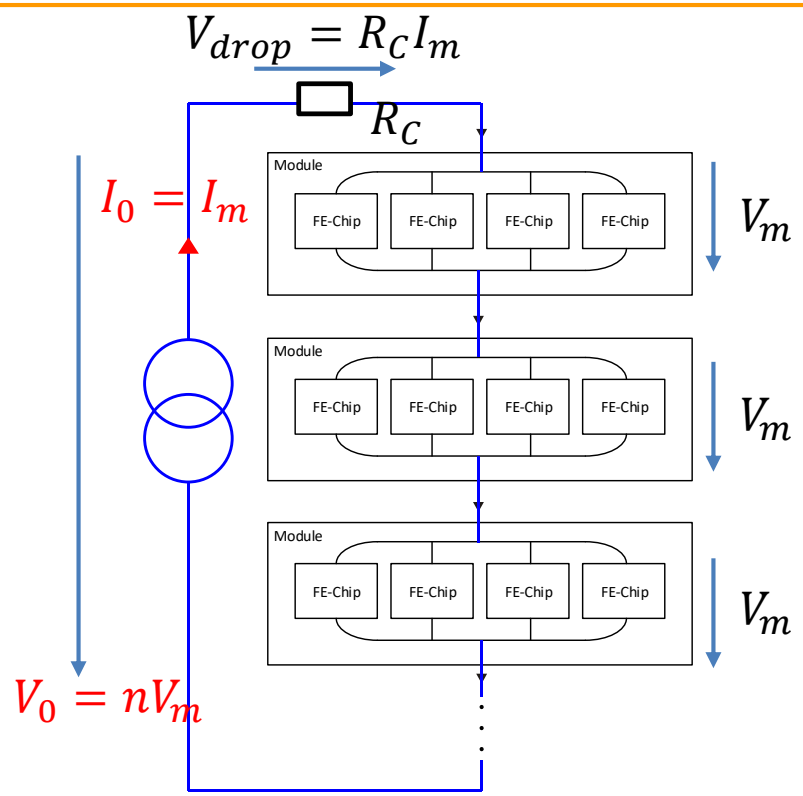


Parallel vs. Serial Powering



- Modules are connected in parallel and powered by a constant voltage source
- Total supply current scales with the number of modules

$$\eta = \frac{1}{1 + n\frac{R_C I_m}{V_m}}$$

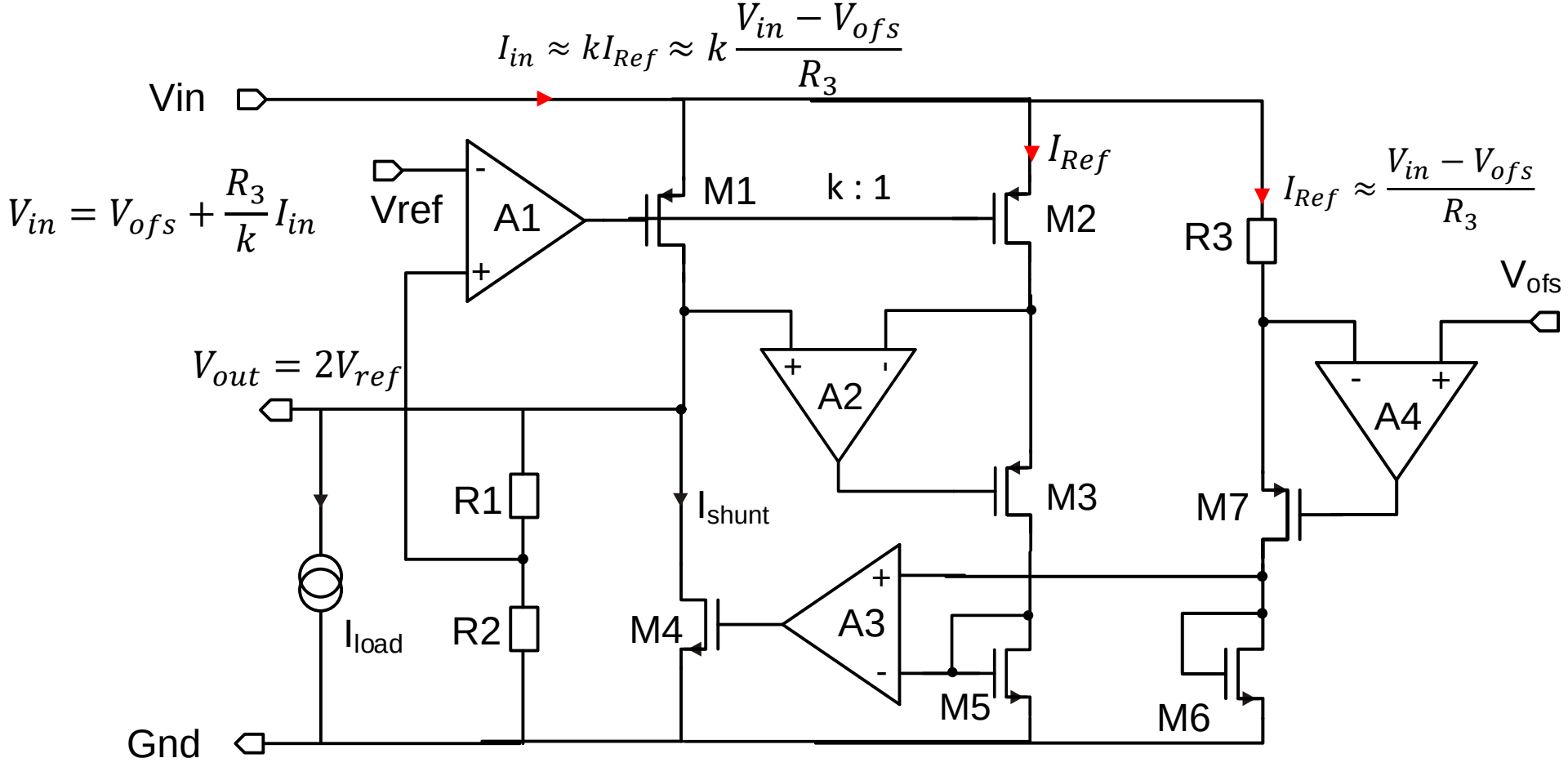


- Modules are connected in series chain and powered by a constant current source
- Total supply current is defined by the highest feasible load current of a single module

$$\eta = \frac{1}{1 + \frac{R_C I_m}{nV_m}}$$

Shunt-LDO Regulator

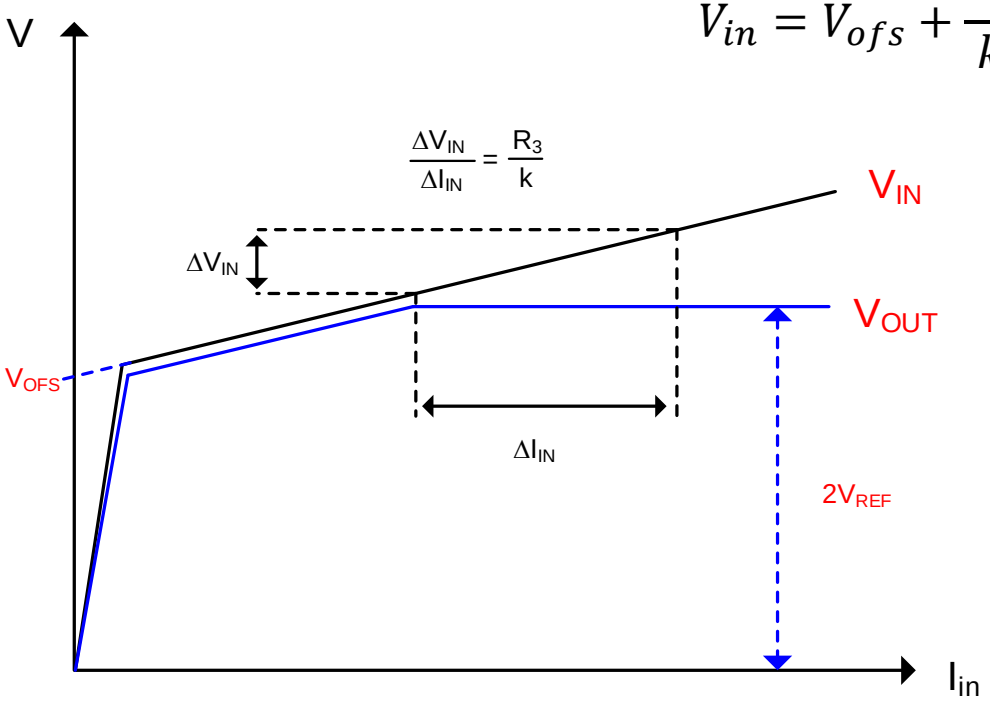
- The Shunt-LDO regulator is a combination of a low-drop-out (LDO) voltage regulator and a shunt regulator
  - Two control loops: 1) constant output voltage 2) constant current flow through the regulator
- Core Transistors are used due to high radiation resistance → carry voltages up to 1.32V
  - Transistors are cascoded for overvoltage capability

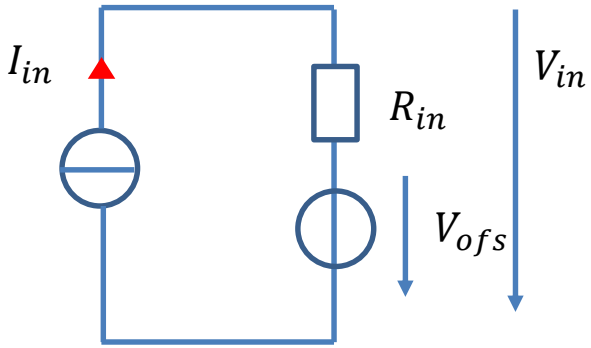


I/V characteristics of the Shunt-LDO

- Shunt-LDO is equivalent to a resistor in series with a voltage source
- Slope is defined by input impedance $r_{in} = \frac{R_3}{k}$
- Output voltage is reached at the point where the amplifier is saturated and the reference voltage is achieved
- The slope of the input voltage ensures a uniform current distribution to parallel regulators

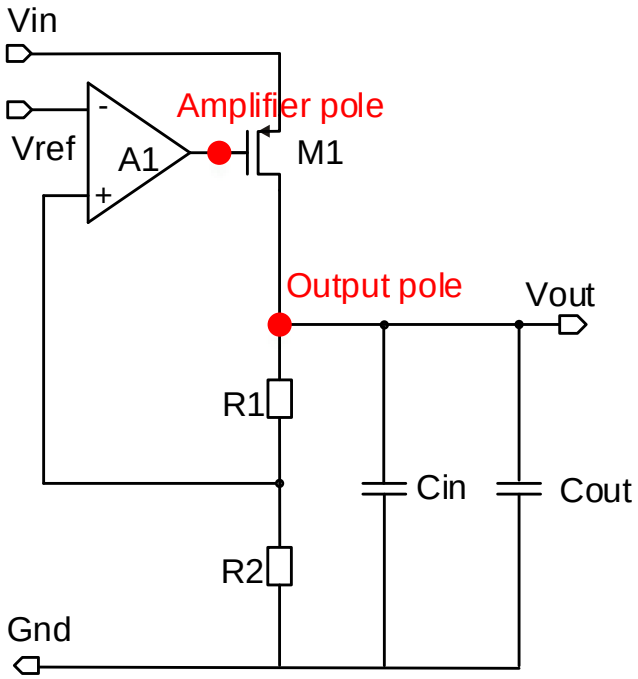
$$V_{in} = V_{ofs} + \frac{R_3}{k} I_{in}$$

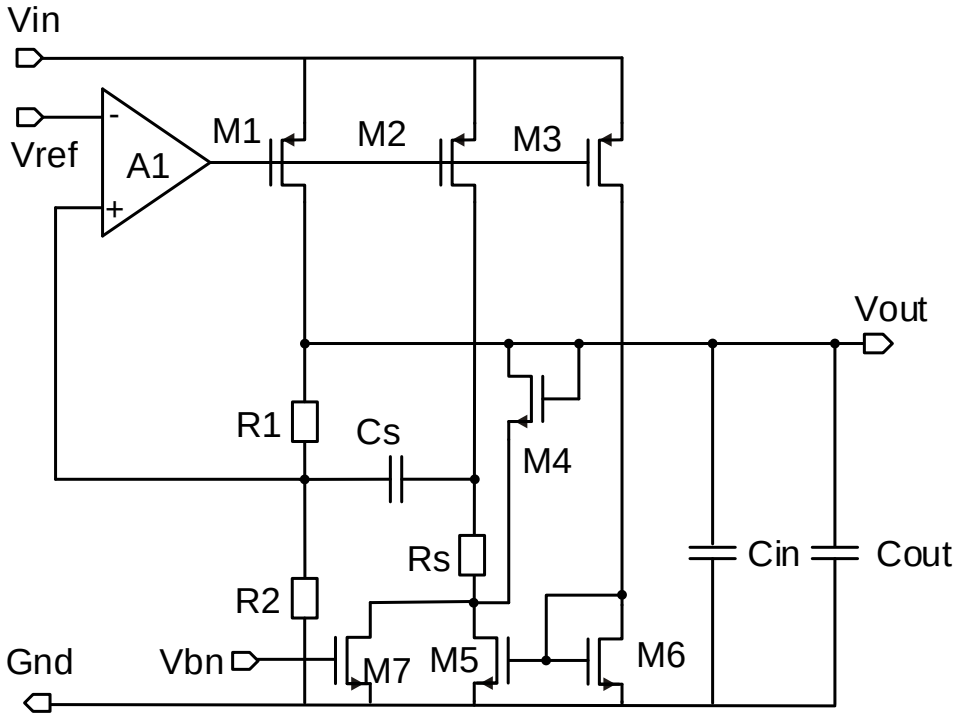




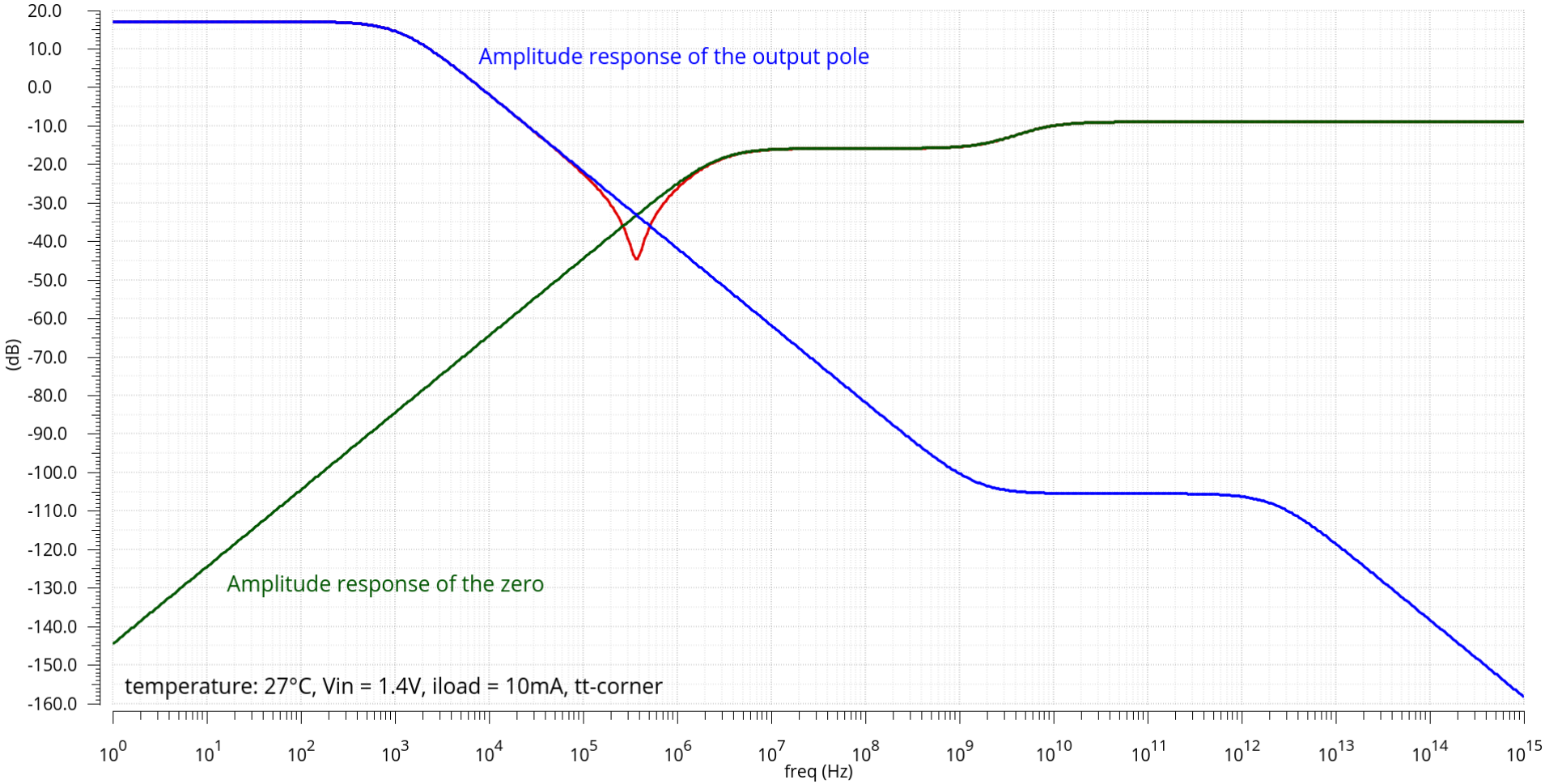
LDO Stabilisation

- The output and amplifier pole will destabilize the LDO
  - A compensation strategy is necessary to insert a stabilizing zero
- ESR compensation is not possible due to the high on-chip capacity
  - On-chip capacitance filters the effect of the zero
- New compensation-scheme:
  - R_S generates a double zero which is coupled into feedback path via C_S





Effect of the Double Zero



- Amplitude response of output pole (blue curve), zero (green curve) and both (red curve)
- First the pole is dominant and at high frequencies the zero
  - Zero dominates at the intersection point with the pole

Determination of the Zeros Frequency

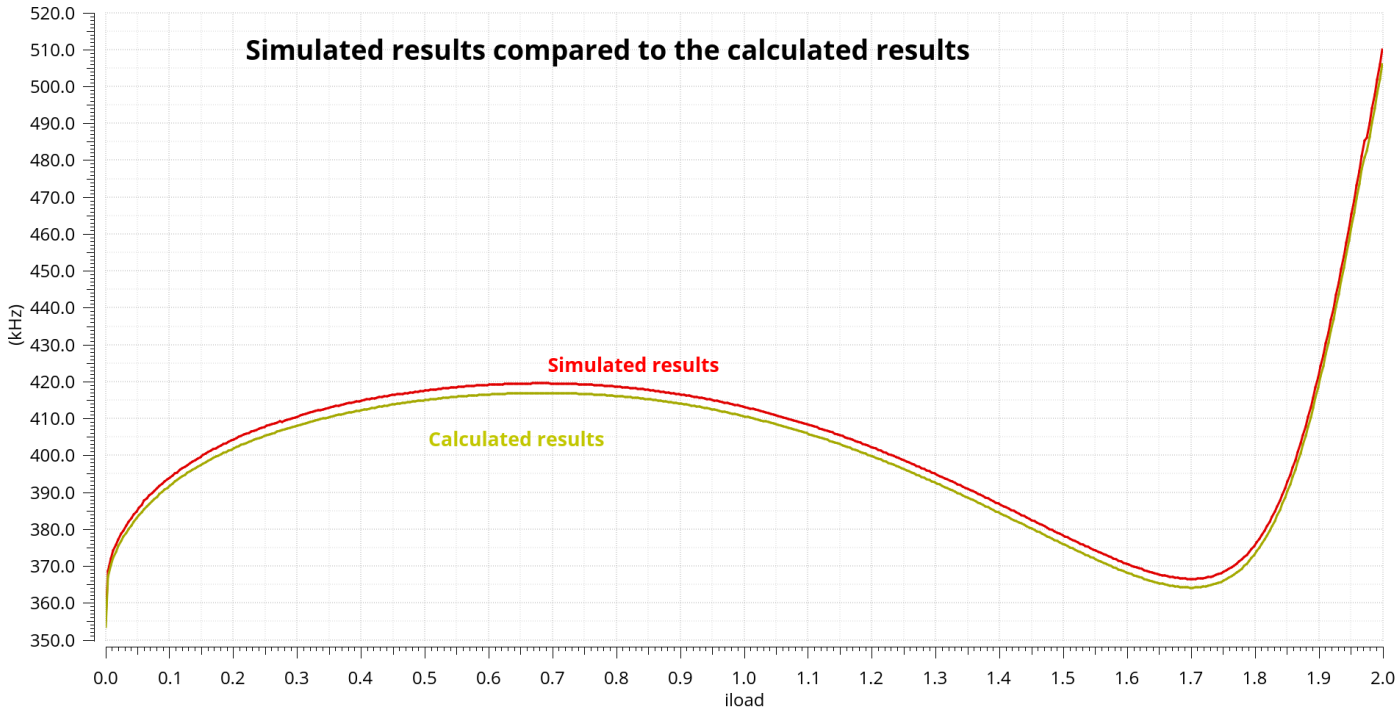
- The frequency of the zero is determined at the intersection with the output pole

$$\omega_z = \frac{1}{\sqrt{2}C_{out}R_{LG}}\sqrt{-1+\sqrt{1+\frac{R_{LG}^4 g_m^2 C_{out}^2}{g_{ms}^2 R_o^2 C_s^2 R_x^2}}}$$

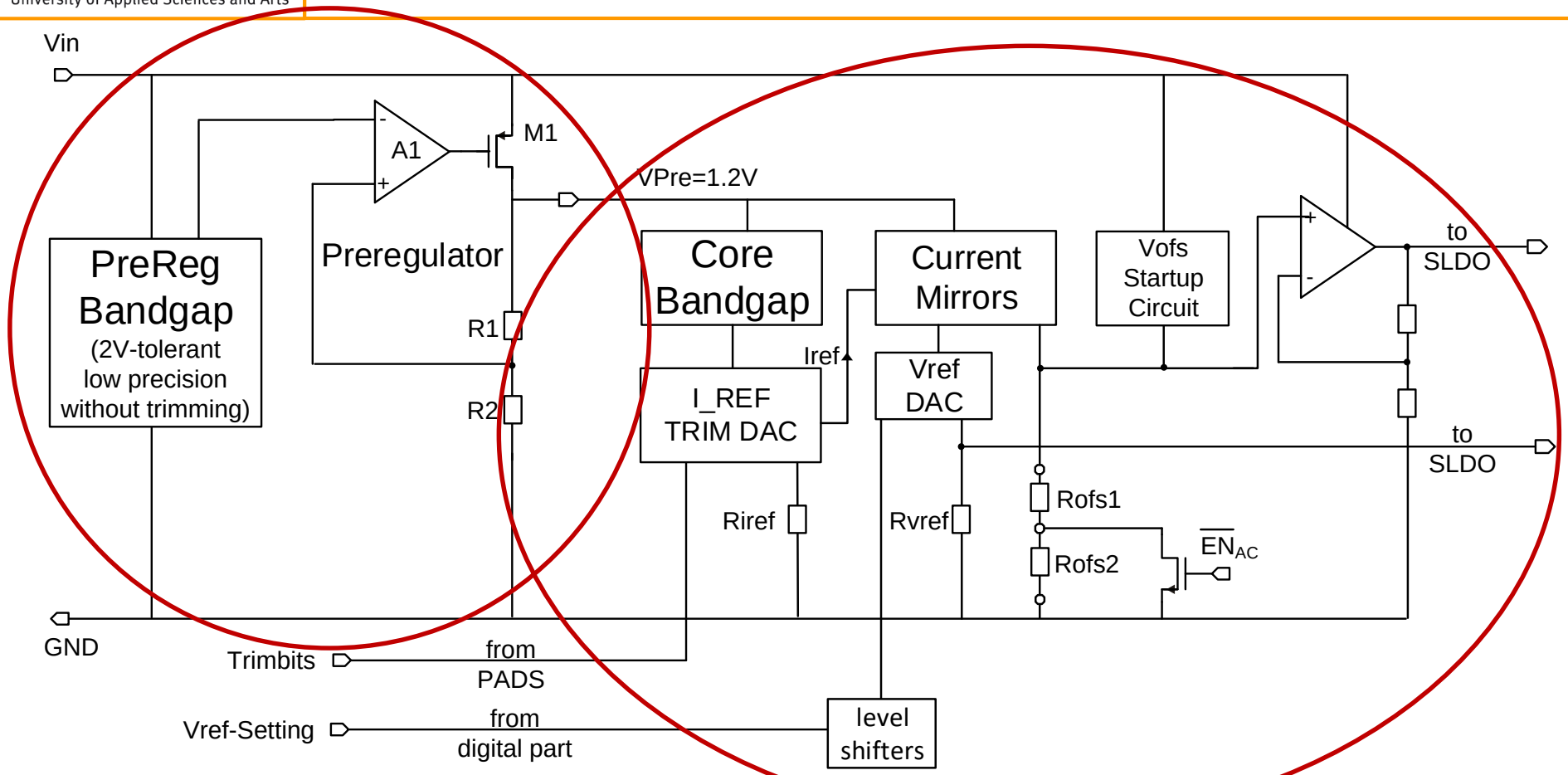
$$R_{LG} = R_{load}||(R_1+R_2)||r_{DS}$$

$$R_x = R_1||R_2$$

$$R_o = r_{DS2}||R_s$$



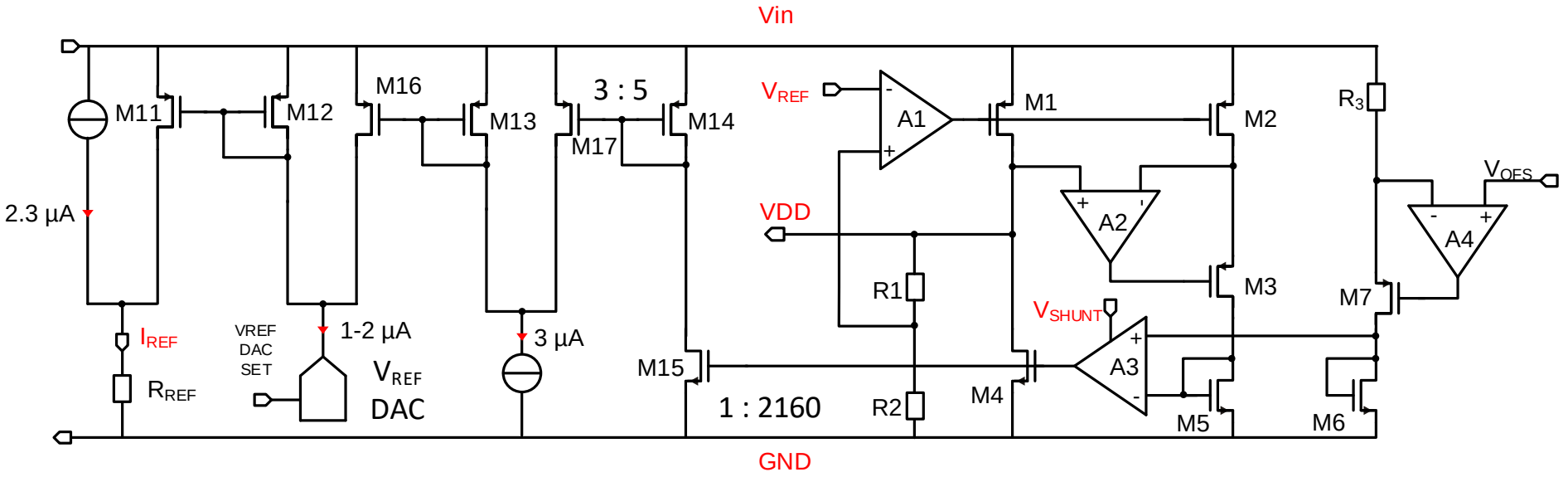
Improved Bandgap Scheme



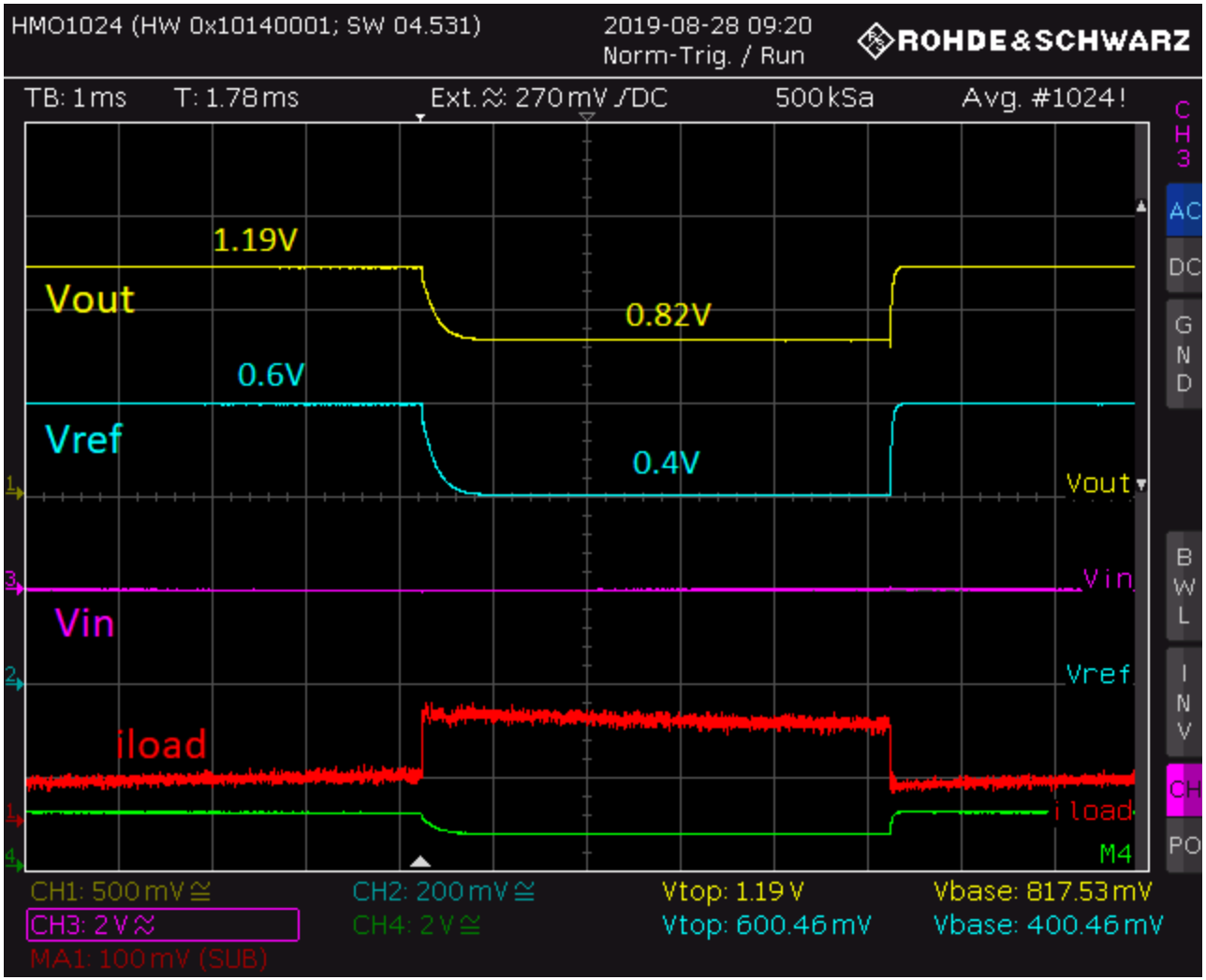
- Two-stage Bandgap scheme
- Pre Bandgap is 2V tolerant and generates a reference for a pre-regulator
- Second bandgap is powered with 1.2V and generates references for the Shunt-LDO
  - More accurate values and the possibility of trimming

Under Shunt Current Protection

- An overload current situation is detected as under shunt current scenario
  - high load current reduces shunt current
- Circuit activates as soon as the current through the shunt transistor is less than 11mA
  - Reference voltage V_{ref} is reduced
- Minimum value for the reference voltage:
  - $V_{ref,min}$ = 150kOhm x 2.3µA = 345mV

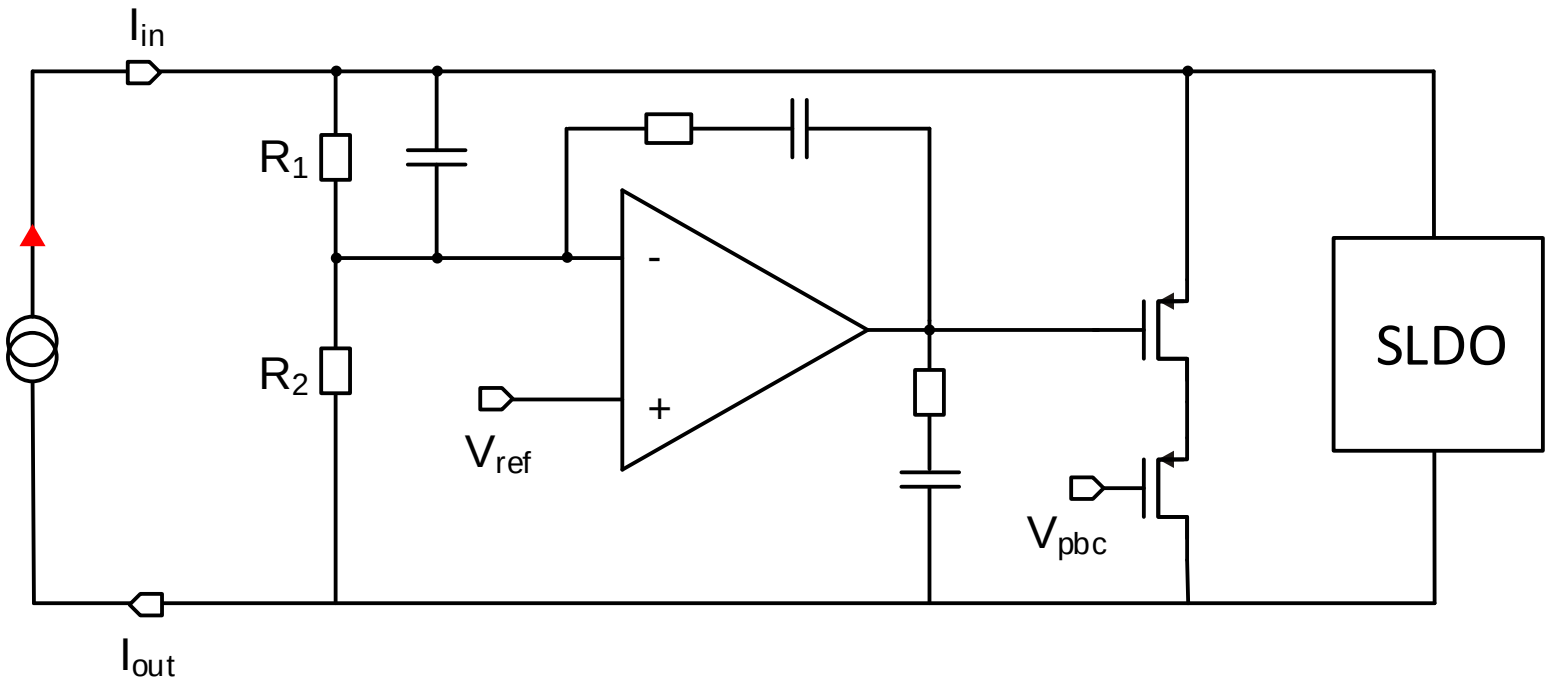


Activation of the Under Shunt Protection Circuit



Overvoltage Protection (OVP)

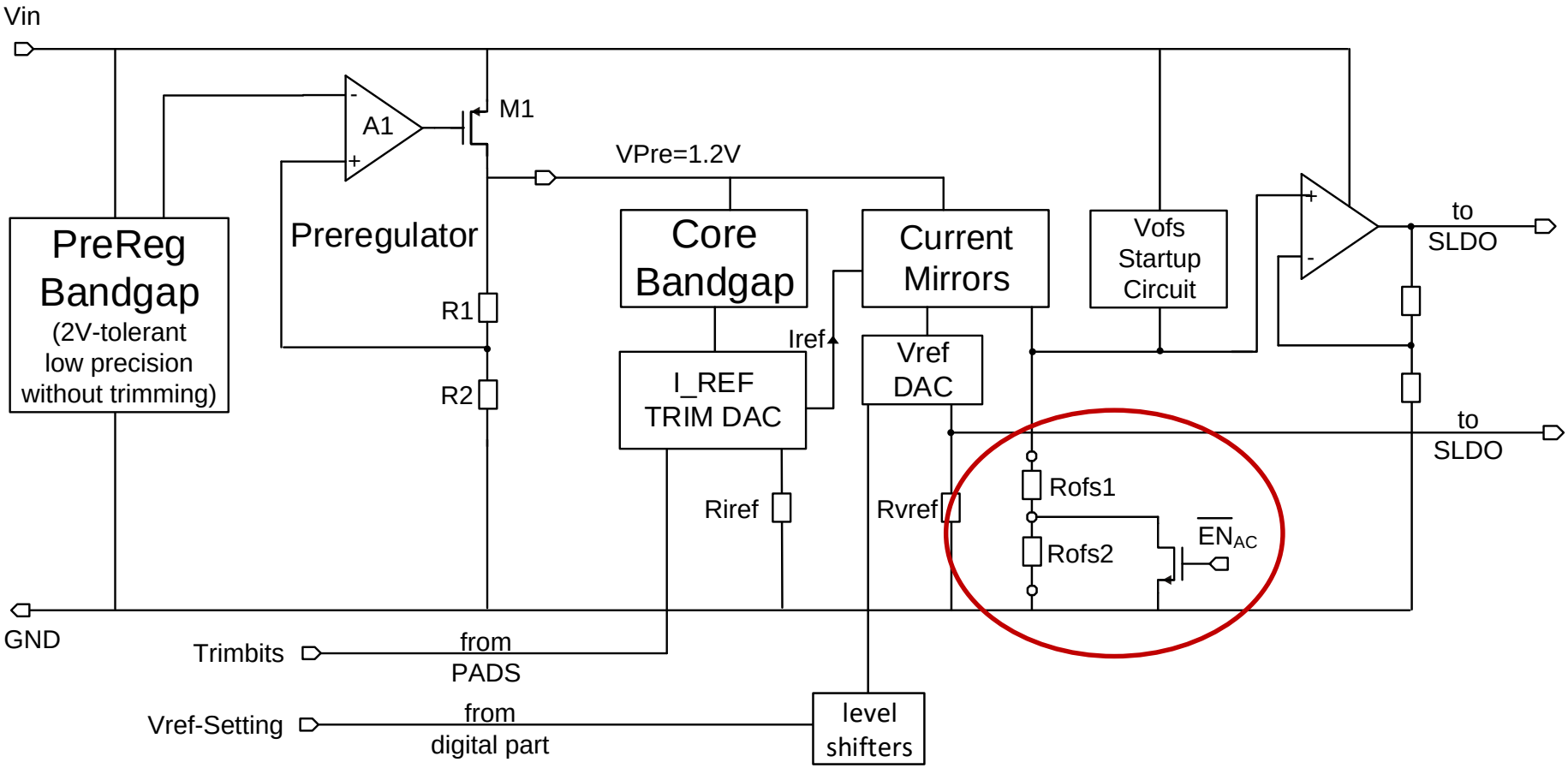
- Protects the regulator from overvoltage
- During an overvoltage situation, the excess supply current is drawn to ground
  - Implemented with a shunt regulator
  - The OVP becomes active if the input voltage exceeds 2V
- Shunt-LDO is connected in parallel to the overvoltage protection



High & Low Power Mode

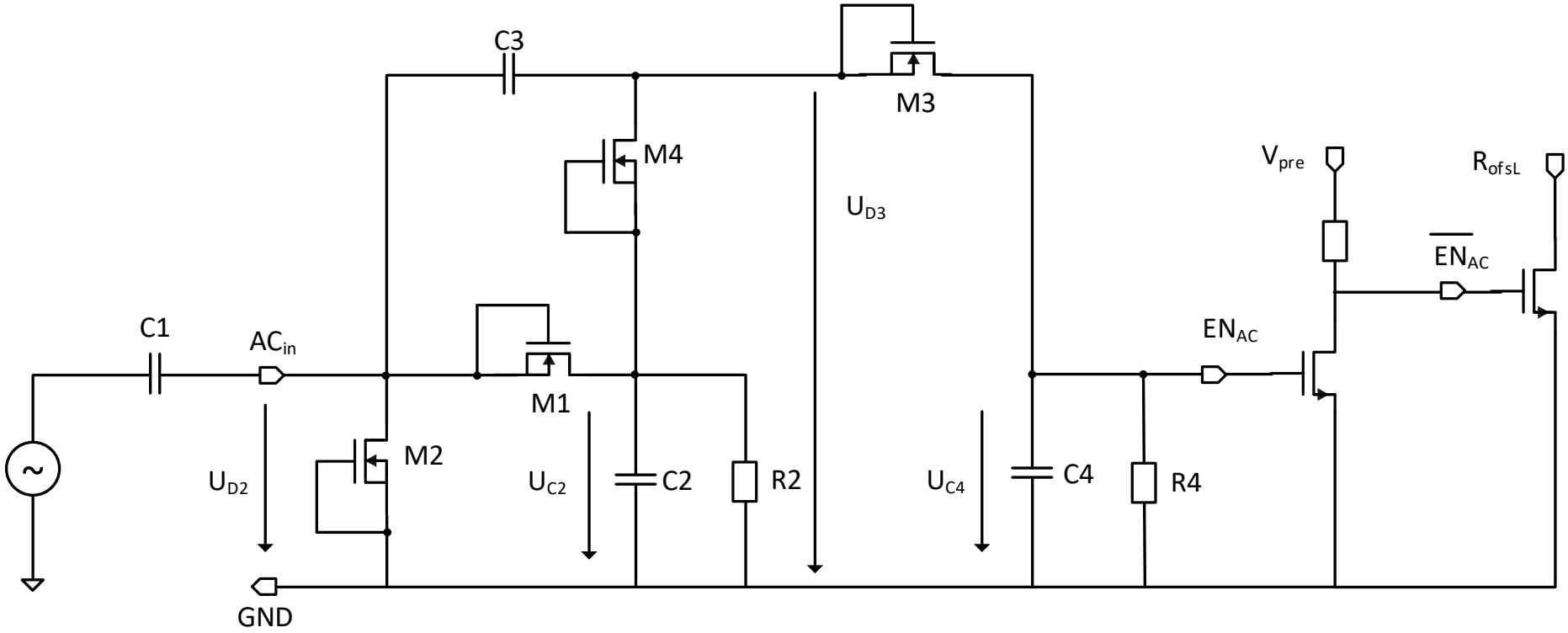
- The regulator operate with low supply currents during the installation phase
  - Since the cooling system is inactive
- Possibility to switch between two Offset voltages
  - High Power Mode is active in the nominal case
    - E.g. V_{ofs} = 800mV
  - Low Power Mode
    - E.g. V_{ofs} is increased to 1.3V
- Start-up circuit is integrated to ensure reliable start-up at small supply currents

Offset Voltage Configuration Capability

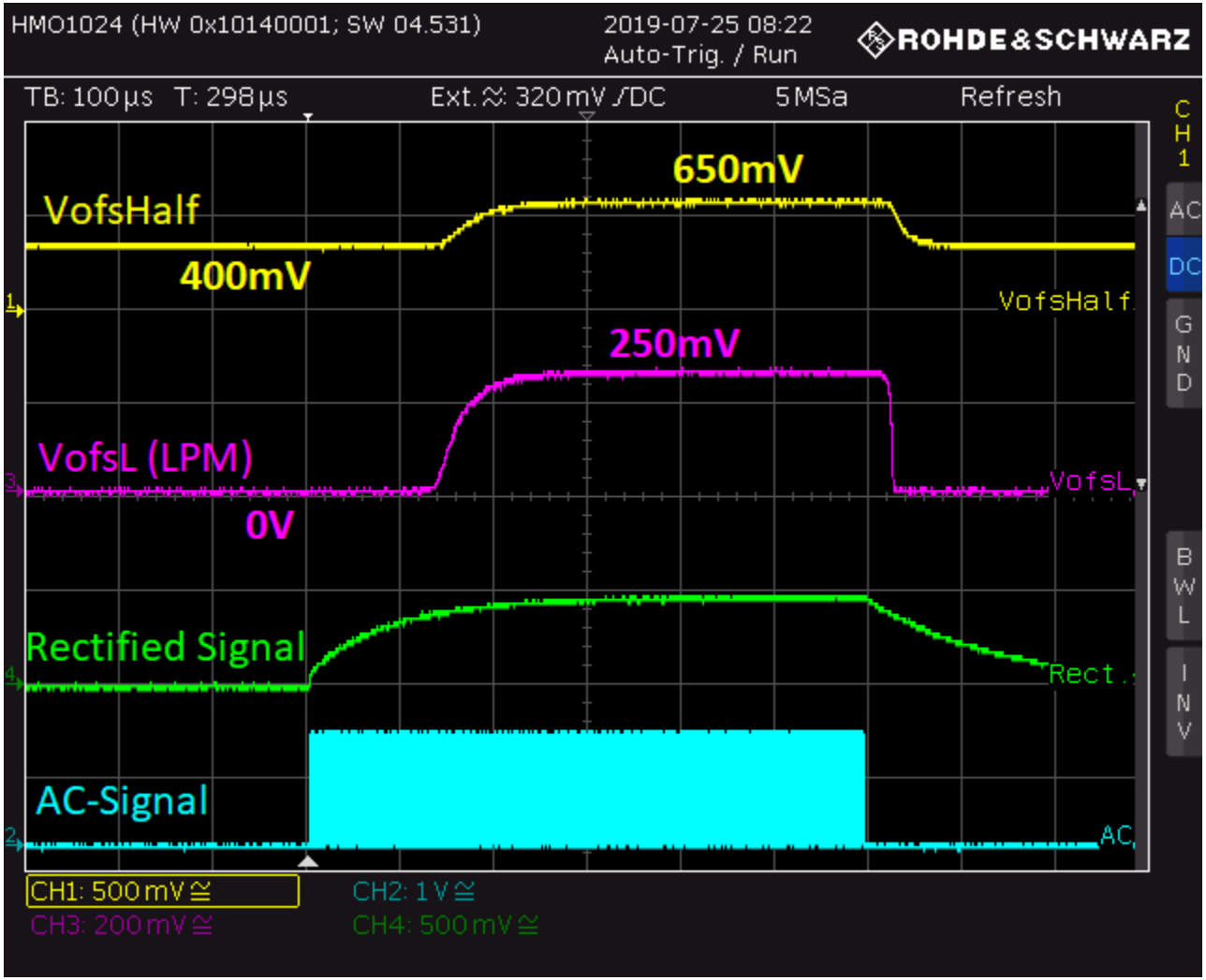


Rectification Circuit

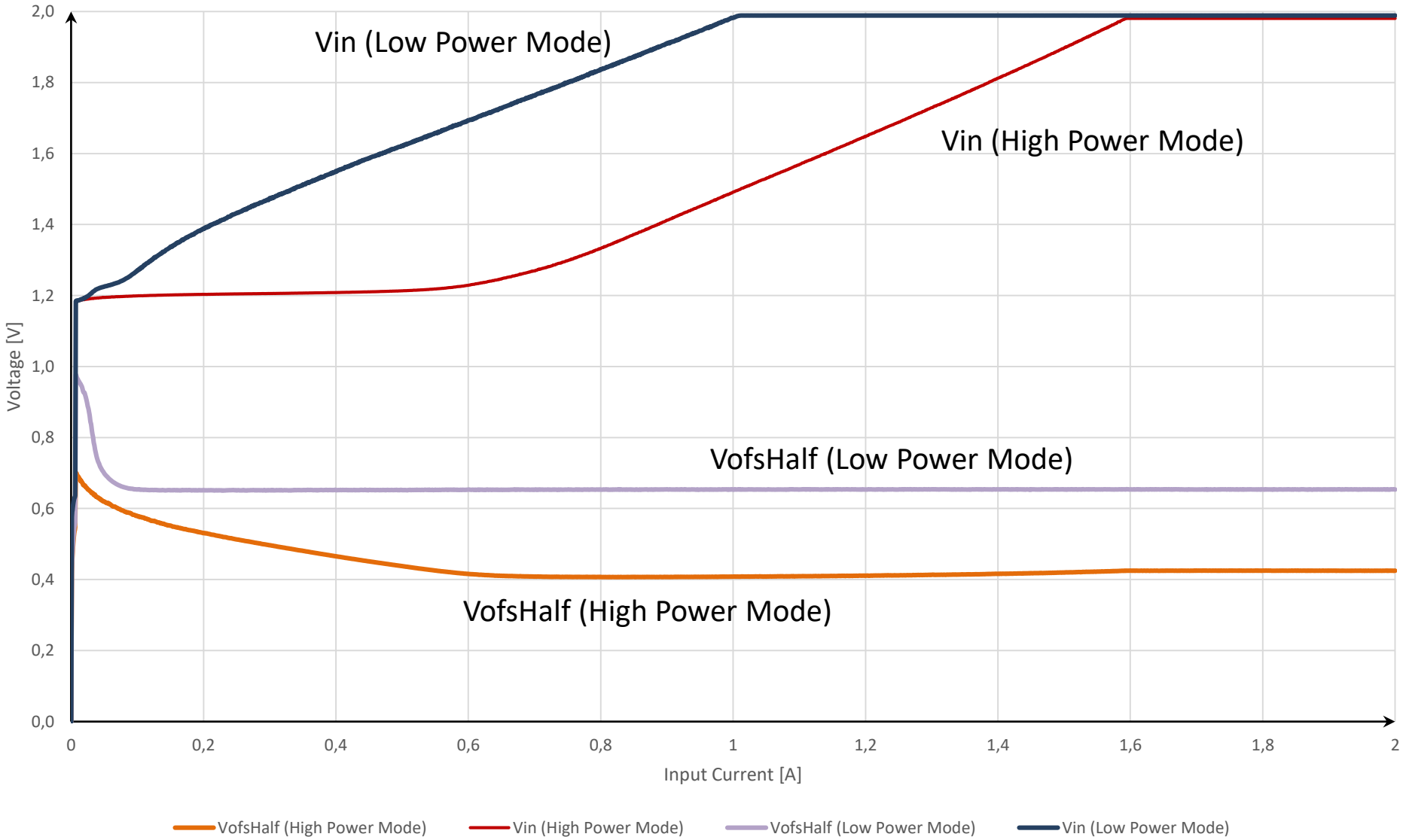
- Inverted rectified signal controls the transistor to switch into the Low Power Mode
- AC signal applied before power on
  - Two-stage rectifier circuit
- Rectifier generates supply voltage for a small digital configuration circuit



Activation of the Low Power Mode



Comparison High & Low Power Mode



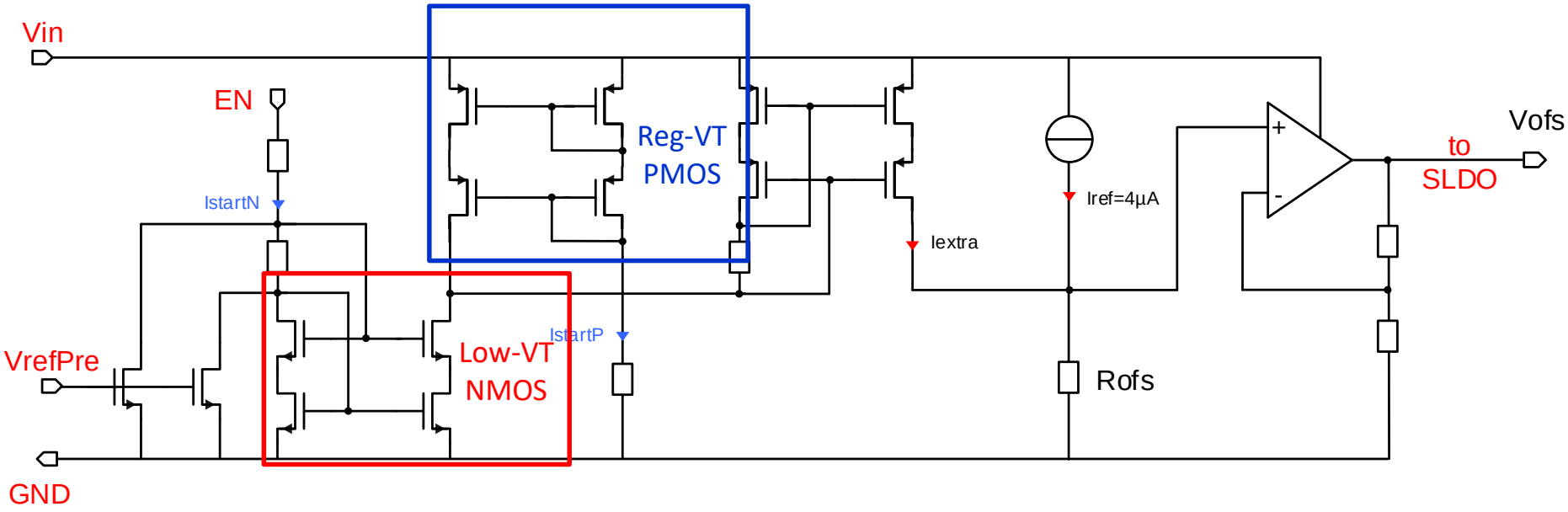
Conclusion

- Conclusion:
  - New compensation scheme stabilizes the LDO regardless of large on-chip capacitance
  - Accurate reference values due to new bandgap scheme
    - Improved PSRR
    - Trimming options
  - Protection circuits were integrated to protect the circuit for overload and overvoltage scenarios
  - The Low Power Mode was integrated for test purposes during the installation phase

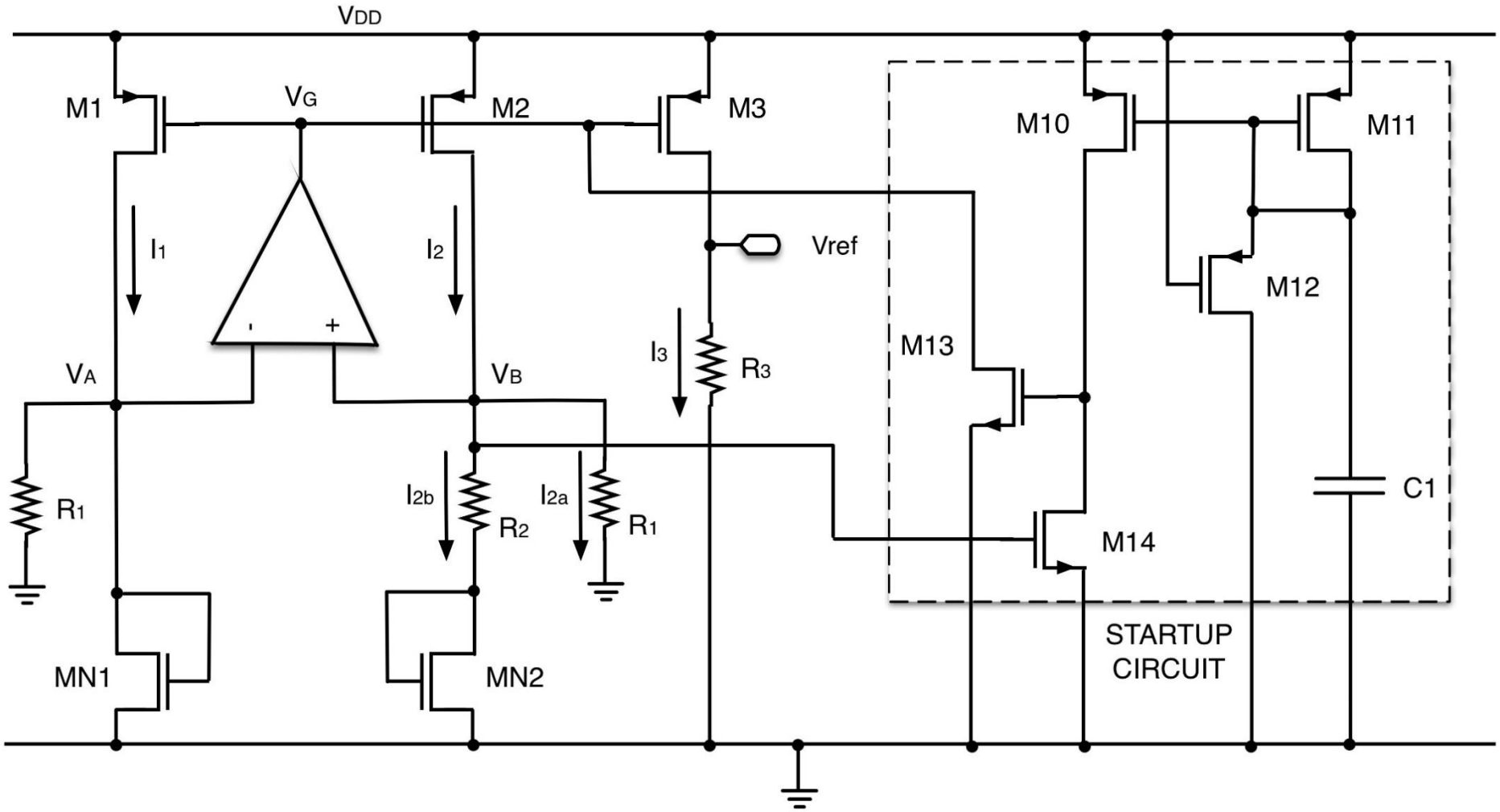
Appendix

Startup Circuit

- Improves start-up behaviour
  - Vofs & Vref follows Vin
- wide-swing cascode current mirror with low-VT NMOS transistors draw current first
- standard cascode current mirror with regular-VT PMOS transistors drain current later
  - difference between current is injected to R_{ofs}



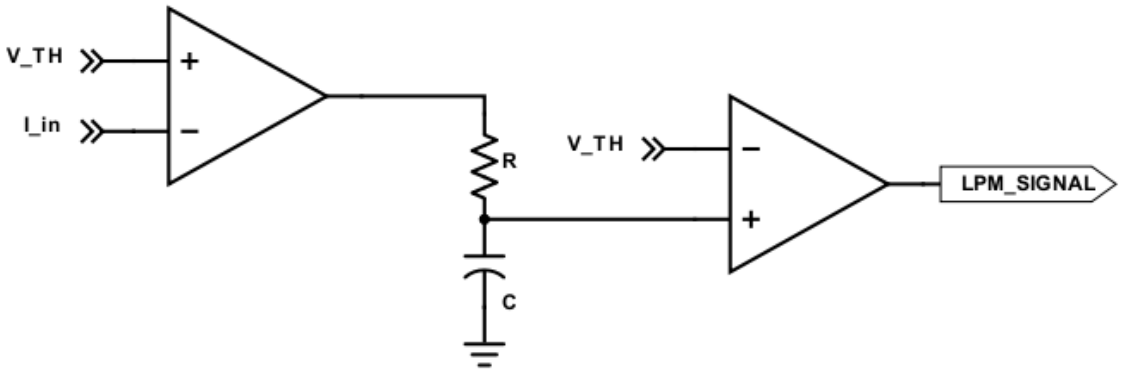
Bandgap Circuit



- Gianluca Traversi: *Characterization of bandgap reference circuits designed for high energy physics applications*

LPM Alvaro Circuit (LPM Signal Generation)

- I_in is measured with a current mirror of the LDO transistor + a resistor.
- If the I_in is bellow the threshold value, a current source is enabled and starts to charge a capacitor (external big capacitor).
- If this capacitor reaches the trigger voltage of the Schmitt trigger, it changes LPM_SIGNAL to HIGH, and LPM is enabled.
- **In case of High Power Mode**, the I_in is going to surpass I_threshold very fast and C1 is not going to be charged at all (in this case this circuit is **almost "transparent" from outside point of view**, without any nasty transient)
- C charging time should be adjusted so that it is slower than the normal start-up time.



- By Alvaro Pradas

Comparison High & Low Power Mode (without activating the Start-up Circuit)