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Stabilization and Protection of the Shunt-LDO regulator for the HL-LHC pixel detector upgrades

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Serial powering is the baseline option for the pixel detectors in both the ATLAS and the CMS experiment targeting the phase II HL-LHC upgrade. The Shunt-LDO regulator is integrated in the front-end chips to generate the required supply voltages. A new compensation scheme has been developed to operate stable with large Low-ESR load capacitances. A two-stage bandgap voltage reference circuit has been implemented to improve regulation performance. Security features have been added to protect against overvoltage and overload. Additional features have been added to allow regulator operation with small supply currents during the installation phase.

Summary

A current based supply scheme of serially connected modules has been chosen as the baseline powering option for the pixel detectors in both the ATLAS and the CMS experiment targeting the phase II HL-LHC upgrade. In this supply scheme the Shunt-LDO regulator is integrated in the pixel front end chips to convert the current supply into the required supply voltages for the analog and digital part. For these regulators parallel operation on chip and module level is required to avoid single points of failure and hot spots to provide redundancy and to increase system reliability. Balanced shunt current distribution across parallel placed devices is reached even if the regulators generate different output voltages by introducing a configurable slope at the Current-Voltage characteristic of the regulator input. The regulator is implemented with cascoded core transistors in 65 nm CMOS technology to tolerate supply voltages up to 2V and high radiation doses at the same time. Due to the large chip size and the large amount of pixels integrated in the front-end chips the regulator needs to deal with a shunt current of up to 2 A and to operate stable even with large Low-ESR capacitances of 300 nF connected to the regulator output. For that purpose, a new compensation scheme has been developed which does not rely on the ESR of the external blocking capacitor which has been successfully applied to the regulator. A two-stage bandgaps scheme has been implemented to improve the PSRR of the regulator reference signals and to reach overall excellent line and load regulation performance. A first untrimmed and 2V-tolerant bandgap reference circuit is supplied by the unregulated input voltages and generates a reference for a linear preregulator. The preregulator supplies a second bandgap reference circuit which is then used to generate the regulator reference voltages. In addition, security features have been integrated which protect against overvoltage and overload conditions. During the installation phase the system will be operated without active cooling. As a result, the regulator needs to startup reliably even with supply currents which are much smaller than the currents reached under nominal working conditions. Therefore a configuration circuit has been developed capable to change the regulator offset voltage which is reached at small input currents. An AC coupled square wave signal is rectified and used as a control signal to change the offset voltage between two values. One value is close to the regulator output voltage for operation with small supply currents and the other value is smaller than the output voltage for efficient operation with large supply currents. For the same reason a startup circuit has been introduced which increases the regulator input impedance and in turn supports the startup procedure. A set of three successive test chips have been produced and tested to validate the proper operation of the circuitry. The newly introduced Shunt-LDO regulator features will be presented together with simulation and measurement results of the produced prototypes.

Authors: Dr KARAGOUNIS, Michael (Fachhochschule Dortmund); KAMPKÖTTER, Jeremias (Fachhochschule Dortmund); Mr STILLER, Andreas (Fachhochschule Dortmund); TRAVERSI, Gianluca (University of Bergamo); PRADAS LUENGO, Alvaro (Aragon Institute of Technology (ES)); KOUKOLA, Dominik (CERN); HINTERKEUSER, Florian (University of Bonn (DE)); ORFANELLI, Stella (CERN)

Presenter: KAMPKÖTTER, Jeremias (Fachhochschule Dortmund)

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