TWEPP 2019 Topical Workshop on Electronics for Particle Physics

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The bPOL12V DCDC converter for HL-LHC trackers: towards production readiness

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We present the electrical and radiation characterisation of the production-ready prototype of the bPOL12V DCDC converter, a stacked assembly of two ASICs inside a QFN32 package. The use of a reference voltage generator chip in 130nm CMOS on top of the ASIC integrating the control system and power train enables improved radiation tolerance and the trimming of the output voltage during the production phase. The comparison of results from proton and neutron irradiations evidence that the NIEL hypothesis is not applicable to the LDMOS transistors used for the bPOL12V, hence making the qualification process for displacement damage more complicated.

Summary

The bPOL12V is an integrated DCDC converter ASIC based on the FEAST2 circuit that has already been deployed in upgraded LHC detector systems, but capable of displacement damage tolerance compatible with the HL-LHC outer trackers'requirements. The electrical specifications generally match those of FEAST2 (maximum power of 10W, with 4A maximum current), with the exception of the input voltage range that might be limited below 12V. Long-term stress tests on fresh and irradiated samples are being conducted at the time of writing this summary, and their result will be presented at the workshop together with conclusions on the maximum recommended voltage.
Similarly to its FEAST2 predecessor, the production-ready ASIC will be distributed in a QFN32 plastic package with thermal pad, but inside the package two ASICs are stacked on top of each other. A small ASIC designed in a commercial 130nm CMOS technology contains a reference voltage generator with excellent radiation tolerance and is electrically connected to the larger bPOL12V ASIC via 3 bond wires. Other than a much better stability of the reference voltage with irradiation, this solution also allows to precisely trim the reference voltage on-wafer for every circuit, ensuring a much narrower distribution of the voltage output of the converter across the full production. This assembly will be tried for the first time in early summer, and results will be presented at the workshop, where we will also describe the full production process starting from the production of the wafers and including the trimming of the reference voltage, the stacked assembly in a single package and the testing.
Samples of the supposedly production-ready versions of the bPOL12V ASIC and of the reference voltage generator will be available for testing in May, and will be exposed to different sources of radiation: X-rays, protons, neutrons and heavy ions. Most of these results, if not all, will be available by September and will be presented at the workshop. Particular relevance will be given to the proton and neutron exposures, since very recent results have evidenced the inapplicability of the NIEL hypothesis for the LDMOS (Laterally Diffused MOS) transistors used in the bPOL12V design. LDMOS exposed in identical conditions at three different facilities (Triga reactor at JSI in Ljubljana, IRRAD at CERN and MC40 at the University of Birmingham) show very different damage when the integrated fluxes are converted in 1MeV-equivalent neutrons. This observation considerably complicates the qualification of the bPOL12V ASICs, since typical specifications for displacement damage tolerance in LHC are reported in 1MeV-equivalent neutron fluxes without indication of the particle composition and energy spectra. A different approach for the qualification is needed, based on measured damage at different facilities and on the precise knowledge of the radiation environment composition at the location where the converters will be installed.

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