RD53A chip susceptibility to electromagnetic conducted noise

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Abstract **- The RD53A read-out chip (65 nm CMOS) is a large-scale demonstrator for ATLAS and CMS phase 2 pixel upgrades. It is one of the key elements of the serial powering scheme for the next generation of pixel detectors. The susceptibility of the RD53A chip with respect to external EM noise has an impact on the integration strategies (grounding and shielding schemes) and operating conditions of future Pixel detectors. This paper presents a detailed analysis of the RD53A chip susceptibility to RF conducted disturbances in order to understand and address noise issues of RD53A Chip before the pixel upgrade installation.**

1- Noise susceptibility tests

- The main goal of these tests is to define the immunity of phase 2 pixel electronics to RF conducted disturbances:
  - ⇒Identify critical elements in prototypes that could reduce detector performance (Grounding, routing, filtering and decoupling).
  - ⇒Noise level limits requirements for the power supply units.
- The results will be used to quantify the impact of different integration options on pixel detector phase II
- Many options / variables have been tested:
  - ⇒Sensor contribution
  - ⇒RD53A FE's: Linear, Synchronous and Differential
  - ⇒Powering conditions: LDO or SLDO mode (Voltage or current power supply)
  - ⇒Analogue or digital domain sensitivity

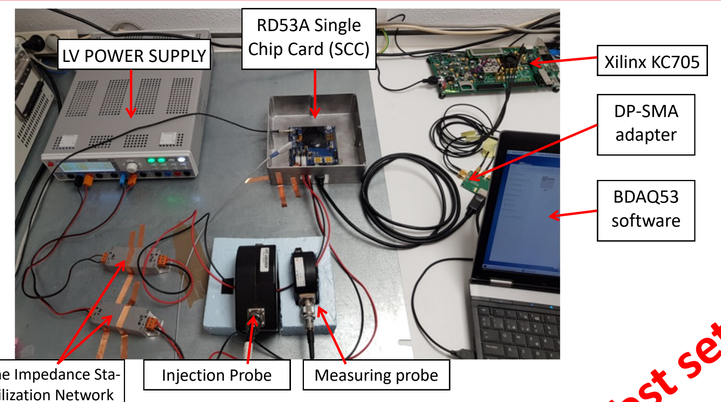
2- How are they performed?

The idea is to inject a perturbing signal to the RD53A chip, and evaluate its impact on the chip performance:

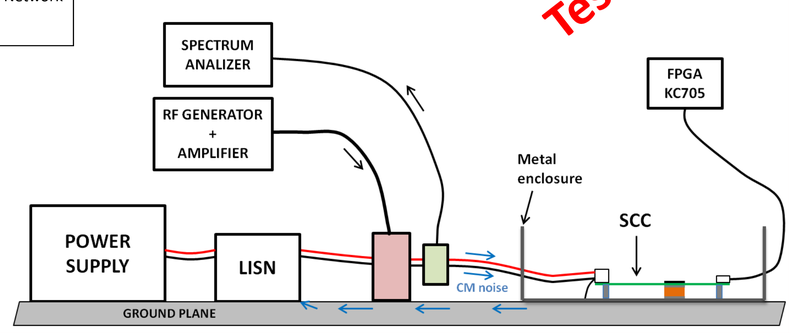
1. **Disturbing current is injected through power lines** using current injection probes:
   - ⇒It is equivalent to conducted noise or coupled radiated field that affects FE modules
   - ⇒Frequency range: 100kHz - 50 MHz
1. RD53A performance is evaluated measuring the average noise (in electrons) using the **Threshold Scan with BDAQ53 readout system**.
2. Having these 2 parameters, the next transfer function can be obtained:

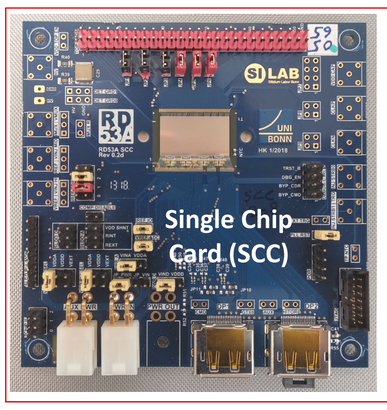
$$TF = \frac{\sqrt{e_{meas}^2 - e_{ref}^2}}{I_{injected}(mA)} = \frac{e_{noise}}{mA}$$

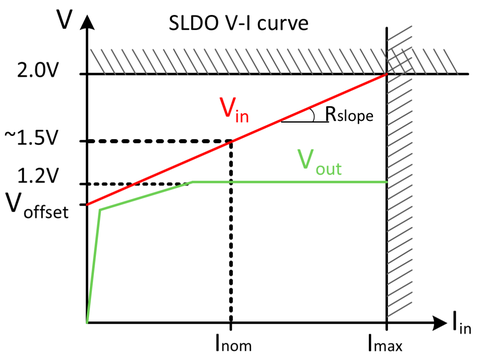
Noise contribution of the injected current on a specific frequency



Test set-up



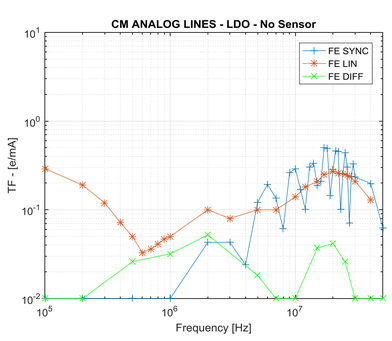




3- Shunt-LDO and Chip configuration

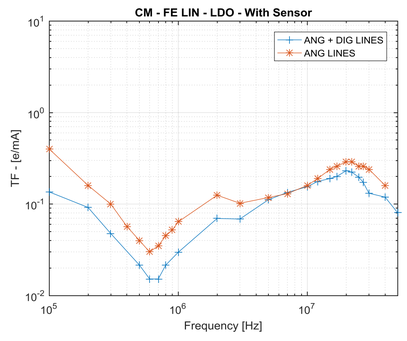
- 2 configurable on-chip shunt-LDO regulators feed separately analog and digital domains. LDO or Shunt-LDO (SLDO) mode can be selected depending on how the chip is going to be powered: with voltage or current (serial powering).
- Two different SCC with exactly the same configuration have been used: one has a bare RD53A chip and the other is a chip + a sensor HLL 25x100um. Chip and SLDO configuration is crucial to get repeatable and reliable results:
  - ⇒Vin of 1.7V is used in both LDO or SLDO mode. SLDO mode is configured with Voffset=1V and R_{slope}~0.7Ω
  - ⇒Decoupling capacitors have been reduced to get designer recommended values: C_{in} = 4x2.2µF and C_{out} = 2x2.2µF
- All FE are tuned to 1100e using designers recommended parameters for each case.

4- FE flavor comparison



- CM noise is injected through the analogue power supply line (LDO mode).
- The response of each Front End is compared:
  - ⇒**Differential FE is the most robust** to noise in all range of frequencies.
  - ⇒Synchronous FE is not affected in <1MHz (AC coupled). It shows the typical response of a sampled signal.
  - ⇒Linear FE is the most sensitive to low frequencies, but better than Synchronous in the high range.

5- Analog and digital domain sensitivity



Two options have been tested in this case:

1. CM noise injection in the analog power lines.
2. CM noise injection in all power lines at the same time (analog+digital)*

The results show, as expected, that **the analog lines are more sensitive to conducted noise**.

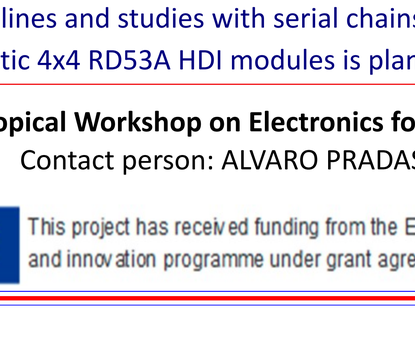
**Separated only digital domain could not be tested due to set-up limitations.*

6- Sensor contribution

Noise susceptibility of the two different SCC is compared using the linear FE. One SCC with just the bare chip and the other with a chip + sensor.

- **The differences are very small**. The presence of the sensor contributes increasing slightly RD53A noise sensitivity.
- This small effect may be caused by the sensor itself generating new noise coupling paths, or just because of having different FE configuration

7- Comparison with FEI4



As a reference, the RD53A TF is compared with the one of FEI4 chip. This is a case of CM noise injection only in analogue power line.

- The results show that **RD53A is less sensitive to injected noise than FEI4**.
- FEI4 was tested with direct powering (no internal regulator) what could explain the big differences, due to the lower PSRR.

8- Shunt-LDO regulator contribution

The noise susceptibility of linear FE is measured for the two powering options, LDO and SLDO.

- **The noise sensitivities are quite different,** mainly at low frequencies (<2MHz).
- This high speed linear regulator (BW > 1MHz) has different control loops per mode, what explains the different frequency response.
- From Virtuoso simulation, the Power Supply Rejection Ratio (PSRR) has a very similar shape compared to noise sensitivity TF.
- These simulations are really useful to identify the link of the decoupling capacitors, parasitic elements and regulator response, with noise sensitivity measurements. Further simulation model studies are ongoing.

9- Summary and future work

- These are the first noise studies of RD53A, but still they give a lot of information:
  - ⇒The results are very consistent and repeatable: good set-up and methodology.
  - ⇒Sensor increases the overall noise sensitivity, but just a little.
  - ⇒The response against noise of each FE is very different. The differential FE is the most robust.
  - ⇒Analogue power line is more susceptible than the digital one as expected.
  - ⇒The regulator makes big impact. SLDO mode is more sensitive than LDO for single chip prototype.
- The results show that RD53A seems to be quite robust to EM conducted noise.
- With this analysis we get a good reference baseline thanks to use a simple prototype. This will allow to understand the contribution of any integration element (grounding, filtering, etc.) included on future realistic prototypes and final detectors.
- Tests of the HV lines and studies with serial chains of SCC are ongoing.
- Testing of realistic 4x4 RD53A HDI modules is planned for the coming months.

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