Contribution ID: **151** Type: **Poster**

RD53A chip susceptibility to electromagnetic conducted noise

Tuesday 3 September 2019 17:20 (20 minutes)

The RD53A read-out chip (65 nm CMOS) is a large-scale demonstrator for ATLAS and CMS phase 2 pixel upgrades. It is one of the key elements of the serial powering scheme for the next generation of pixel detectors. The susceptibility of the RD53A chip with respect to external EM noise has an impact on the integration strategies (grounding and shielding schemes) and operating conditions of future Pixel detectors. This paper presents a detailed analysis of the RD53A chip susceptibility to RF conducted disturbances in order to understand and address noise issues of RD53A Chip before the pixel upgrade installation.

Summary

The extreme high rate operation of the ROC at the HL-LHC requires the use of 65nm high density low power CMOS technology with low working voltage (1.2V), resulting in a pixel chip that must be supplied with significant current levels (˜2A per chip). During the last years, extensive studies have shown that a serial power distribution system is the only feasible scheme to supply the pixel detector with the required power within an acceptable material budget and power cable losses.

From the point of view of electromagnetic interferences (EMI), there are no precedents of this type of powering scheme on a high energy physics detector. In a serial powering scheme, each power group has several modules connected in series and fed with constant current. From the Grounding/EMC point of view this topology is characterized by having only one module connected to the system ground, and the rest floating at different potential levels. In order to avoid EMI problems and define a good grounding strategy, it is important to quantify the noise sensitivity of RD53A chip against EM conducted noise. For that purpose, noise currents at different frequencies are injected with current probes through the power lines of the RD53A chip (both low and high voltage), and then the equivalent noise charge (ENC) per channel is measured. The ratio between the measured noise and the perturbing injected current is used to compute the transfer function of RD53A chip against EM conducted noise.

This paper shows the first part of the EMC studies of RD53 chip to identify potential noise issues and critical elements. EMC tests have been performed using Single chip cards (SCC) prototypes based on RD53A in order to analyze chip configuration, and component level implications (input/output filter characteristics). Several topologies and options have been tested: SCC with and without sensor, analog front-ends (Synchronous, Linear and Differential) and powering conditions, LDO mode (powered in voltage) and Shunt-LDO mode (powered in current). This set of tests will be used on future stages (serial power chain based on SCC and HDI EMC tests) as a reference to quantify the effects of integration strategies on the susceptibility of pixel detector against EM noise.
This is the first time that this kind of tests and analysis has been performed in a readout chip prior to its final integration. The outcomes of this study will allow understanding the coupling mechanisms of electromagnetic noise associated to read-out chip. The resulting susceptibility profiles provide emission requirements for noise sources in the experiment, as well as grounding and shielding guidelines for CMS pixel phase II. This information will help system integration designers to enhance the robustness of the pixel system, and therefore its integration in the whole experiment.

Authors: PRADAS LUENGO, Alvaro (Aragon Institute of Technology (ES)); ARTECHE, Fernando (Instituto Tecnológico de Aragón); ESTEBAN LALLANA, Maria Cristina (Aragon Institute of Technology (ES)); Dr ARCEGA, Francisco (Universidad de Zaragoza)

Co-authors: CHRISTIANSEN, Jorgen (CERN); SILVA JIMENEZ, Ester Maria (Universidad de Cantabria and CSIC (ES)); KOUKOLA, Dominik (CERN); ORFANELLI, Stella (CERN)

Presenter: PRADAS LUENGO, Alvaro (Aragon Institute of Technology (ES))

Session Classification: Posters

Track Classification: Power, Grounding and Shielding