A High Throughput Production Scale Front-End Hybrid Test System for the CMS Phase-2 Tracker Upgrade


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Outline:

1. Introduction
2. Requirements of the test system
3. Backplane and test card designs and performance
4. Firmware and software
5. Conclusion

CMS: Compact Muon Solenoid
The CMS Tracker Phase-2 Upgrade is required to adapt the CMS Tracker to the 3000 fb$^{-1}$ total integrated luminosity and 14 TeV centre-of-mass energy of the HL-LHC.

Two main module types are being developed for the upgrade. The readout electronics are based on flexible hybrid circuits assembled on Carbon Fibre (CF) reinforced stiffeners for both modules.

**HL-LHC**: High Luminosity Large Hadron Collider; **2S**: Strip-Strip module; **PS**: Pixel-Strip module;
Different hybrid types and foreseen quantities

Many different hybrid types and variants for the upgrade:

- 4 main types and 3 spacing variants for the PS modules = 9* different types
- 3 main types and 2 spacing variants for the 2S modules = 6 different types

<table>
<thead>
<tr>
<th>2S module</th>
<th>Quantity required [pcs]</th>
</tr>
</thead>
<tbody>
<tr>
<td>2S front-end hybrid 1.8 mm; 4 mm left and right variant</td>
<td>2x 8750 + 2x 550</td>
</tr>
<tr>
<td>2S service hybrid 1.8 mm; 4 mm</td>
<td>8750 + 550</td>
</tr>
<tr>
<td>Total 2S type hybrids to be tested</td>
<td>27900</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PS module</th>
<th>Quantity required [pcs]</th>
</tr>
</thead>
<tbody>
<tr>
<td>PS front-end hybrid 1.6 mm; 2.6 mm; 4mm left and right variant</td>
<td>2x 990 + 2x 1750 + 2x 4000</td>
</tr>
<tr>
<td>PS readout hybrid 1.6 mm; 2.6 mm; 4mm variant</td>
<td>990 + 1750 + 4000</td>
</tr>
<tr>
<td>PS power hybrid common</td>
<td>6740</td>
</tr>
<tr>
<td>Total PS type hybrids to be tested</td>
<td>26960</td>
</tr>
</tbody>
</table>

* The three different spacing variants can be merged in one hybrid design for the PS power hybrid.
Introduction of the hybrid circuits

Closest real life prototype

- 8CBC3 prototype (2S front-end hybrid)

- 2S service hybrid*

3D model of final hybrid

- 3D model of the 2S front-end hybrid

- 3D model of the 2S service hybrid

PS type

- PS-MCK prototype (PS front-end hybrid)

- PS readout hybrid prototype is in production

- PS power hybrid prototype*

- 3D model of the PS front-end hybrid

- PS readout hybrid 3D model

- PS power hybrid 3D model

* These two hybrid prototypes were developed by RWTH Aachen.
The hybrid circuits are:

- High Density Interconnect (HDI) flex circuits reinforced with CF stiffeners.
- Dielectric layers are 25 µm thick with 9 – 21 µm copper.
- Smallest line width and spacing is 42.5 µm.
- Via laser drill is 25 – 50 µm in diameter in a capture pad of 110 µm - 125 µm.
- Vias are filled with copper and staggered to increase reliability.
- Up to 3000 (PS) or 6000 (2S) signal interconnections in one circuit.
- Up to 6500 bump bonds on front-end hybrids.

**Cross sectional view of the PS front-end hybrid.**

**Cross sectional view of the 2S front-end hybrid.**

HDI: High Density Interconnect; MPA: Macro Pixel ASIC; SSA: Short Strip ASIC; CIC: Concentrator ASIC;
Electrical testing is an essential part of the quality check procedure:

- Hybrid level electrical test is required to verify that all the critical bump bond connections and passive component connections are present.
- Short finding and antenna tests are required to verify that there are sufficient number of channels operational in the hybrid under test and it’s quality is satisfactory for module construction.
- Functional testing is required to prove that no ASICs were damaged during the assembly procedure.
- Tests are essential to achieve a good yield in the module assembly.
Requirements for the test system and design choices:

- High throughput enables testing at manufacturer -> Multiplexing
- Scalability to reduce installation costs at collaborators - > Modular backplanes
- Compatibility with already developed hardware and software - > Usage of FC7
- Versatility to support test card for each hybrid type - > USB bus and LVDS IOs
- Usage of standard elements where possible - > Commercial cables and sub sub-rack

Standard 3U size 19-inch sub-rack was selected to host the test cards.

Interconnection is through the commercially available Samtec HDR cables.

Data acquisition is done through the FC7 FPGA board.

**HDR**: High Data Rate cable. Sub-rack is compliant with IEC 60297-3-101. The 3D model is based on Atos 2300179 (frame).
Highlights of the backplane design:

• By interconnecting three backplane cards a full. Each backplane has selectable address.
• Only one plug in card can be active at the time. Power switch must be on the plug-in cards, backplane sends the card select signal. 1.4V and 3.3V are provided to the plug-in cards.
• Up to 16 high speed input and 43 output signals are multiplexed. Signals with direction to the plug-in cards (inputs) are buffered. USB bus is multiplexed as well.

Three interconnected backplanes forming a full-size backplane. Front (left) and back (right) side 3D model of a single backplane unit.

Backplane layout and schematic was designed by Rafael Gajanec.
Multiplexing and buffering

- Multiplexing is in a tree arrangement with TS3DV642 1:2 multiplexers. Low power consumption and a bandwidth up to 7.5 GHz.
- High speed signals with direction to the plug-in cards are buffered with the DS25BR LVDS buffer. Possibility of pre-emphasis or larger swing.

Backplane multiplexing scheme

Multiplexing scheme of input signals with additional buffering

Multiplexing scheme of output signals. Buffering is on the plug-in cards.
The design concept was validated by measurements of the multiplexer chain with 3 m twinaxial cable and 1 m of PCB stripline with the DS25BR buffer.
Component performance eye diagrams

Eye diagram measured with the setup on the previous slide @ 640 Mbps without buffering.

Eye diagram measured with the setup on the previous slide @ 640 Mbps with buffering and pre-emphasis.
Backplane layout

- Level 1 multiplexers
- Card select and card present logic
- Backplane interconnection connectors
- USB and power connectors
- Reverse polarity protection

Buffers, only enabled when backplane is selected
Plug-in card slots
Power good logic
Address selection DIP switch
Level 2 and 3 multiplexers
Based on S parameter measurements at the module 2 slot 0 including a 3 m long twinaxial cable, eye diagram simulations showed good signaling performance at 1.28 Gbps (unbuffered). Performance at higher rates can be sufficient.

Buffered signals have larger eye opening, both are sufficient for standard LVDS receivers.
Plug in cards, cables and strain reliefs fit mechanically as expected.

All the slots of the backplanes are operational with the 2S test card, the same test results are obtained in all positions.

Plug in card powering works correctly. Card selection, backplane selection logic works as expected, power good signals are also working correctly.
USB-SPI bridge for peripheries: ADC, switches, potentiometer
ADC for voltage and temperature measurements
LVDS buffers
Antenna test switches for analogue input connectivity test
Samtec SEAM right angle high data rate connector
Power jumpers for crate usage
Power connector for standalone usage
Flex adaptor with fine pitch connector
CIC mezzanine support
8CBC3 hybrid prototype
Specific aluminium socket to host 8CBC3 prototypes
Status LEDs

2S test card layout and schematic was designed by Paolo Baesso.
Signal performance on the 2S test card

Eye diagram of the 320 MHz clock line on the 2S test card after buffering (FC7->3m HDR cable-> 3 backplane units -> 2nd test card slot.)
• The 2S test card was designed to be operational in stand-alone mode as the IO mapping is compatible with the FMC VITA standard.
• The card operates correctly in the stand alone mode with 8CBC3 + CIC mezzanine (2S hybrid from data point of view).
• The card is compatible with future 2S hybrids, left and right side as well.
The PS hybrid testing is more complicated than the 2S as the MPA is missing from the data chain at the tests.

A spring loaded needle probe socket (POGO) is needed to test the SSA output signals. A pusher mechanism is also required.

Number of IO signals is insufficient to test all the chips in one go, therefore only two SSA chips are tested at the time.

Communication through main connector as in the module.

CIC inputs will be generated by test vectors.

SSA chips are multiplexed in pairs to test inter-chip communication.

Only the hybrid is tested.
PS test card mechanical design and socket

- Pusher element forced by pivot lever
- Bottom pusher plate with spring washers
- Hybrid POGO test socket
- Place of hybrid pusher insert with inverted profile
- Backplane connector

PS test card layout and schematic currently being designed by Angelos Zografas.
The PS-ROH test card design uses two FC7 FPGA boards. One to test the signals communicating to the front-end circuits, and one to test the back-end communication through the optical links.

PS-ROH test card layout and schematic is being designed by Nikola Rasevic.
PS-ROH test card design

- USB to SPI communication block
- PS-ROH under test
- VTRX+ connector
- LpGBT
- Buffers and signal translation
- Backplane connector

- PS-ROH hybrid spacer height adaptor
- Height adaptor with rugged connector
• The development of the 2S service hybrid test system was started by RWTH in Aachen. A compatible test card with the crate based test system will be developed for production scale testing.
• There is no test card design for the PS power hybrid. A test card is planned to be developed for this purpose.
• Some mechanical elements are still under development or not developed. Some of the flexible cables are still need to be manufactured.
• The crate based hybrid test system uses a core FC7 firmware that assures the proper usage of the hardware. This core firmware is the same for all test cards.

• Each hybrid test setup requires a modified firmware image where the specific IO functions are mapped and other test functions are added.

Firmware development by Jarne De Clercq, Mykyta Haranko, Inna Makarenko.
• The main test functions such as: calibration, I2C register read and write, short detection, antenna test etc. are all integrated in the Ph2-ACF middleware. The middleware will be used in the future tests to integrate all test functions.
• The communication between the computer and the FC7 is through the IPBus protocol. The test results, calibration data and configuration details will be stored in a common database.
• Many different hybrid prototypes are being developed for the CMS Outer Tracker Phase – 2 Upgrade.

• To electrically test the large quantity of hybrid circuits needed for the upgrade, a versatile, high throughput test system is required.

• A high speed modular backplane was developed to multiplex the hybrid test cards.

• Test cards are developed for the PS, 2S and PS-ROH hybrids. The 2S test card was successfully tested.

• Specific firmware is developed for the test system, each hybrid test card requires specific firmware version.

• The Ph-2 ACF middleware contains all the test tools used for the hybrid testing.

• Software and firmware development is in progress, new test cards need to be developed for the 2S service hybrid and the PS power hybrid.
Thank you for the attention
Backup PS Pogo socket design

- Pusher element forced by pivot lever
- Bottom pusher plate with spring washers
- Hybrid POGO test socket
- Place of hybrid pusher insert with inverted profile
- Alignment pins

Spring probe contact placed in the designed socket