Contribution ID: **72** Type: **Oral**

A High Throughput Production Scale Front-End Hybrid Test System for the CMS Phase-2 Tracker Upgrade

Friday 6 September 2019 09:00 (25 minutes)

More than twenty-five thousand hybrids will be produced for the CMS Tracker Phase Two Upgrade. The hybrids are assembled with flip-chips, passives and carbon-fibre stiffeners. They will be glued to their module supports, together with powering and optical transmission hybrids, making repairs almost impossible. Due to the complexity of the hybrid circuits and the circuit assembly, production scale testing is a very important aspect. A crate-based scalable test system was designed to enable a multiplexed test of front-end hybrids. A test card was produced for the 2S hybrids and two different hybrid test cards are under development.

Summary

Ten different front-end hybrid variants for the Compact Muon Solenoid (CMS) Tracker Phase Two Upgrade for the High-Luminosity Large Hadron Collider (HL-LHC) are currently under development. The upgraded Tracker is based on two main types of modules, the strip-strip (2S) and the pixel-strip (PS). The 2S modules contain two parallel strip sensors of 10 × 10 cm2 and two front-end hybrids connected to a service hybrid. The PS modules contain a strip sensor and a macro pixelated strip sensor of 5 × 10 cm2 and two front-end hybrids connected to a power and a data service hybrid. These modules require state of the art High Density Interconnect (HDI) front-end hybrids assembled with fine pitch flip-chip front-end ASICs, connectors and passives.
The 2S front-end hybrids interface through a fine pitch connector with a service hybrid that contains the power conversion and a Versatile Link Plus (VTRX+) based optical link connecting to the back-end systems. The PS hybrids have an additional interface with a Macro-Pixel Sensor ASIC assembly block (MAPSA) which is located externally. The proposed system tests the hybrids through these interfaces.
The test infrastructure is based on a 3U 19-inch sub-rack with custom developed multiplexer backplanes enabling the testing of twelve hybrid circuits in one crate. The backplanes are designed to multiplex high speed differential signals, USB, control lines and distribute power. Each sub-rack can fit three backplanes interconnected in series enabling the test with twelve hybrid plug-in cards. In this scheme, smaller systems can be assembled as well, down to four plug-in cards. The backplane connects to the FC7 data acquisition board, which controls the selection of plug-in cards and processes the data. The FC7 is connected through IPBus to a computer running the test software. Performance of the backplane was characterized and validated for up to a clock frequency of 640 MHz.
Specific plug-in cards are designed to test each main type of hybrid circuit. In order to avoid designing ten different plug-in card variants, the hybrids are mounted on interchangeable sockets and specific interconnection circuits are designed to connect them to the plug-in cards. The first edge card was designed for all six variants of the 2S hybrids. The card was qualified with the 8CBC3 prototype hybrid linked to a mezzanine hosting the concentrator ASIC (CIC). Two other test cards are currently under development to test the PS optical readout hybrids (PS-ROH) and the PS front-end hybrids.

The proceeding will present the design and topology of the test crate and the 2S test card. Results obtained with the 8CBC3 and the CIC Mezzanine will be shown. The design of the PS test card including the hybrid socket design will be presented. The test case for the PS-ROH hybrid will also be presented.

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Session Classification: Production, Testing and Reliability

Track Classification: Production, Testing and Reliability