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LpGBT Tester: an FPGA based test system for the lpGBT ASIC

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The lpGBT transceiver is a radiation tolerant ASIC designed to be used in High Energy Physics detector systems. It aggregates data from up to 28 eLinks to one high-speed link running at 5.12 or 10.24Gbps. In the downlink direction, it can be used for timing and trigger distribution by demultiplexing the incoming downlink bitstream running at 2.56Gbps onto up to 16 eLinks. Moreover, the lpGBT provides additional interfaces to handle the detector slow control. This paper presents the lpGBT tester, based on a Xilinx development kit and a custom FMC card developed to perform the pre-production test.

Summary

Following the lpGBT design, started in 2015, the first batch of LpGBT was produced and delivered at CERN by the end of 2018. The specification defines the transceiver chip interfaces: bi-directional high-speed links to be connected via optical fibre to the back-end electronics, up to 28 electrical links (eLinks) to receive detector data and 16 eLinks to transmit trigger and configuration information to the front-end modules. Elinks are grouped in groups and can be configured with different data rates: 80, 160, 320Mbps for the downlink and 160, 320, 640, 1280Mbps for the uplink. Additionally, the lpGBT delivers 32 clocks with configurable frequency of 40, 80, 160, 320, 640 or 1280MHz. Besides eLinks, the LpGBT offers several slow control features: ADCs, voltage DAC, current DAC, temperature sensor, I2C masters, and GPIOs.

The lpGBT tester is based on the VC707 evaluation platform from Xilinx and a custom dual-port FMC card featuring an lpGBT dedicated socket. A complete and flexible Python framework was developed to streamline the process of testing various functionalities of the chip. The software communicates with the FPGA through an Ethernet interface using the IPBus protocol. The lpGBT-FPGA IP core is instantiated in the firmware to handle the high-speed link. Numerous multimode eLink serializer and deserializer, emulating detector component, were developed to perform complete Bit Error Rate test. The test system offers a set of functionalities to check the slow control features using internal logic or communication with external analog devices.

The development process is based on the Gitlab's continuous integration and issue reporting features to ensure the working state of the main project and split de workload among the developers. Therefore, every time a new feature is implemented and pushed to the remote repository, the software and firmware are compiled and tested on a target platform before being merged to the master development branch.

This paper presents the tester's hardware, firmware and software modules as well as the development workflow used to improve the development reliability.

Primary authors: MENDEZ, Julian Maxime (CERN); BARON, Sophie (CERN); BIEREIGEL, Stefan (BTU - Branderburg University of Technology (DE)); DE OLIVEIRA FRANCISCO, Rui (CERN); FONSECA, Jose; HERNANDEZ MONTESINOS, Daniel (GBTx - BE Group); KULIS, Szymon (CERN); PORRET, David (CERN); RODRIGUES SIMOES MOREIRA, Paulo (CERN)

Presenter: MENDEZ, Julian Maxime (CERN)

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