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Qualification of the final LHCb VELO electronics

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The Vertex Locator of the LHCb will be upgraded in 2020. As the installation is approaching all the electronics have to be verified and tested. In this poster, the final test setup for all the components and the procedures accomplished will be described. Problems detected and solutions adopted will be explained.
This process goes from visual inspection test of the different boards or bare Asic qualification to a full system test with the final components. The auxiliary boards and specificly designed firmware to properly facilitate the testing will be illustrated.

Summary

The LHCb Vertex Locator will be fully replaced by a new pixel detector in 2020. This new detector is composed of 208 sensors bump bonded to 624 VeloPix Asics (3 Asics per sensor). All these Asics are wire-bonded to 208 hybrids and controlled by 104 GBTx Asics using another specific hybrid. These hybrids are interconnected with 208 flex tapes using 832 connectors (4 each tape) and placed with high precision on a silicon substrate together with the tiles (1 sensor + 3 VeloPix) that are used as a support and as micro-channel CO2 cooling. The VeloPix Asics readout signals and the GBTx control signals are transmitted via 208 flex tapes divided in two segments: one with low mass in the acceptance area made of micro-strip lines and another made of ˜0.5 metre strip-lines. These readout flex cables are connected to the hybrid using 728 connectors and have to be able to transmit 5.13 Gbps signals. The flex tapes are connected to a Vacuum Feed-through Board and which are then connected to an Opto and Power Board.
Due to the quantity of sensors, Asics, and boards required and the inability to replace most of the components after the installation, precise systematic tests have to be done for all the detector components at each production and assembly step. This poster presents an overview of all tests performed as well as the qualification process accomplished. The problems found and the solutions adopted will be explained. First, the full Asic qualification procedure before and after bump bonded and the results obtained are presented. Second, the visual inspection of all the hybrids and flex cables is described in order to spot any problems that could affect the high speed signal transmission. Third, the tests made on all the boards in terms of high speed communication are illustrated. TDR or eye diagram measurements are used for this test with the help of specifically designed auxiliary boards. Finally, a slice system test is described mentioning the problems found when all the fully tested and validated components are join together.

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