“Increased radiation tolerance of CMOS sensors with small collection electrodes through accelerated charge collection”
a.k.a.
“first results from the MiniMALTA demonstrator”

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CMOS detectors

- a quick recap: the MALTA chip
  - design
  - results

- learning from the results: the Mini-MALTA prototype
  - design
  - results
(one of) the next challenges for pixel detectors

- Upcoming colliders (HL-LHC, FCCह) will run at very high instantaneous luminosities:
  - $8-30 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$
  - significant amount of pileup (200-1000) interactions per bunch crossing

- Large hit rate: 200 MHz/cm$^2$
  - need small pixel to separate individual particles

- Very large radiation dose:
  - HL-LHC pixel detector: $2 \times 10^{16} - 1 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2 \text{ NIEL}$
  - current LHC detectors needs to be replaced at the end of Run3
Hybrid silicon detectors:
- most popular technology in current large scale detectors
- well known technology with proven radiation hard properties
- reasonably expensive and custom process

Monolithic CMOS:
- industrial-like production: suited for large area detector
- small segmentation to maintain low occupancy in high particle flux
- potential for low material budget and low power detector
- still in R&D phase (in particular for what concern radiation hardness)
✦ Successfully implemented for the ALICE ITS
✦ Small collection electrode —> small input capacitance
✦ Small depletion depth: 25-30 µm
✦ modified process with additional low dose n-type implant:
  ✦ achieve full lateral depletion
  ✦ improve radiation hardness
✦ typical bias voltage: 6 - 20 V (substrate), 6V (pwell)
- 22 x 20 mm² full size demonstrator
- **512 x 512 pixels**
- 8 sectors with different pixel flavours
- **Fully clock-less matrix architecture**
- Charge information from time-walk
- 10 mW/cm² digital power

- Pixel size: 36.4 x 36.4 µm²
- 2-3 µm² collection electrode:
  - *small input capacitance: few fF*
- 3.5-4 µm spacing to electronics:
  - *low cross talk*
- 1 µW/pixel analog power:
  - **70 mW/cm² digital power**
MALTA: front end

Operating principle derived from ALPIDE front end
D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042

Charge measurement from time difference between bunch crossing time and leading edge of hit signal (no ToT)

timewalk <25 ns for Q>300 el

Typical performance (before irradiation):

- $th \sim 250 \text{ el}$, $RMS \sim 35 \text{ el}$, $ENC \sim 7 \text{ el}$
Novel asynchronous readout architecture for high hit rate capability with 40 bit parallel data bus for data streaming:

- Groups of 2x8 pixels with pattern assignment to reduce data size from clusters
- Front-end discriminator output is processed by a double-column digital logic
- Pulse width adjustable between 0.5 ns and 2 ns
- Data transmitted asynchronously over high speed bus to end of column

At the periphery, arbitration and merging resolves timing conflicts of simultaneous signals [currently disabled]:

- Timing information stored in dedicated bits
- Output signals transmitted by 5 Gbps LVDS driver
- one MALTA word consist of 38 bits

Custom chip readout implemented in Virtex VC707:

- asynchronous oversample of parallel 38 lines
- measuring hit arrival time with 400ps precision
**First submission [*]**: delivered in Jan 2018
- pixel readout and pixel pulsing functional
- slow control not fully functional -> partial masking only on double column level, no individual pixels
- hit merger in the periphery disabled due to too high noise activity can cause data collisions at very hit rate

**Second submission (MLVLC) [*]**: delivered in Jun 2018
- MLVLC = Metal Last Vias Last Change
- Improve connections to digital power in the slow control block
- Improve PWELL connections in the matrix
- Chip behavior remained similar to first submission

**Third submission (MALTAC)**: delivered in Febr 2019
- fully functional Slow Control capabilities at reduced digital voltage

[*] chips irradiated up to $1e15 \text{ n}_{eq}/cm^2$
Analog signal properties

Threshold scan measurements

Test beam campaigns at SPS:
- April-October 2018
- MIMOSA-based telescope: 2 µm resolution
- both unirradiated and samples irradiated up to 1e15 n_{eq}/cm²
- preliminary results presented last year by B. Hiti
- a quick recap in the next slides
**Test beam results**

**high threshold:**
- inefficiency for low signals (charge sharing)
- low noise

**low threshold:**
- higher sensitivity for low signal
- significantly larger noise
- lack of pixel masking produce inefficiency due to hit merging

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Unirradiated
(W6R6, )

93.6 % — 97.1 % — 96.2 %

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Irradiated
5x10^{14} n_{eq}/cm^2
(W6R21, )

55.1 % — 71.1 % —

Decreasing threshold, from ~600 e⁻ to ~250(unirr)/350(irr) e⁻

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Clear inefficiency seen after irradiation

Dao Valerio

TWEPP 2019
In pixel efficiency: overlay of many pixel groups

Unirradiated (W6R6, S3)

Irradiated \(5\times 10^{14} \text{n}_{\text{eq}}/\text{cm}^2\) (W6R21, S3)

Decreasing threshold, from \(\sim 600\ e^+\) to \(\sim 250\text{(unirr)/350( irr)}\ e^+\)

Couldn’t reach lower threshold

Inefficiency are mainly originating at the corner of the chip
Test beam results

Inefficiency are mainly originating at the corner of the chip

✦ Efficiency after irradiation drops more in the corners
✦ Center of the pixel is affected by merging at lower thresholds
✦ Corners of the pixel improve with lower threshold
✦ no strong dependence on substrate voltage in range 6-15 V
**Effect of the p-well structures**

- Inefficiency structures inside the pixel correlated with deep PWELL distribution
- Inspired modifications discussed with the foundry and effort on TCAD simulation
- Proposed modification of the PWELL structure at the chip boundary to water the field configuration

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**Sector 2**
Max deep p-well

**Sector 3**
Med deep p-well

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Modified process:

**Modified process with additional p-implant:**

**Modified process with gap in n-layer:**
- 5 x 1.7 mm² demonstrator
- 64 x 16 pixels with 36.4 µm pitch
- based on the MALTA pixel front-end with key improvements
- 8 sectors with different analogue front-end design, reset mechanism and sensor implant process
- different SlowControl implementation
- periphery data synchronization using a custom RAM memory
- single serial data stream: 40Mbs or 1.2 Gpbs with 8b10b encoding

Mini-MALTA wire-bonded on a carrier board
Increased size of transistors to reduce RTS noise:

- M6: x2 larger
- M3: 20% larger
Process modification inspired by TCAD simulation

**Before irradiation:**
- Modified process
- Modified process with additional p-implant
- Modified process with gap in n-layer

**Total current [A]:**
- Particle incident at 1ns - 6 V

**Particles:**
- M. Munker, Pixel 2018

**After irradiation:**
- Modified process
- Modified process with additional p-implant
- Modified process with gap in n-layer

**Total current [A]:**
- Particle incident at 1ns - 6 V
- Irradiation dose of $10^{10}$ neq/cm²

**Modified Process:**
- NWELL
- PWELL
- DEEP PWELL
- LOW DOSE N-TYPE IMPLANT
- DEPLETED ZONE
- DEPLETION BOUNDARY

**Standards:**
- S0
- S1
- S2
- S3
- S4
- S5
- S6
- S7

**Standard, PMOS reset:**
- extra-deep p-well
- n- gap
MiniMALTA: threshold scan

✦ (for the same configuration) enlarged Nmos front end shows *significantly lower threshold and smaller pixel-by-pixel dispersion*

✦ enlarged transistors front end has *smaller average ENC and significantly smaller ENC tails*

✦ noise ~double after irradiation

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*More information on Poster from Lluis Simon Argemi*
intermezzo: MALTA telescope

- testbeam in ELSA: 2.5 GeV electrons

new beam telescope made entirely of MALTA(C) planes:
- 2 arms (3 planes each) + 1 plane inside the cold box
- flexible trigger schema (up to 3 planes coincidence)
- precise region of interest capability (also in trigger)
- high rate capability [up to few kHz] with low per-event occupancy (~1 hit)
- achieving 14 µm track-hit resolution using only 3 tracking planes and General Broken Line (GBL) algorithm in Proteus
- similar performance as MIMOSA telescope in DESY
Efficiency map in Mini-MALTA

(99.7 ± 0.1)%
(99.7 ± 0.1)%
(99.6 ± 0.1)%
(99.7 ± 0.1)%
(99.1 ± 0.1)%
(98.9 ± 0.1)%
(97.9 ± 0.1)%

very high and uniform efficiency before irradiation
visible improvement in efficiency from modifications:

✧ ~13% improvement due to new transistor
✧ ~6% improvement from process modification: similar improvement from deep p-well and n-gap
Efficiency map in Mini-MALTA: summary

✧ for $1 \times 10^{15}$ $n_{eq}/cm^2$:
  ✧ efficiency stably above 97% for threshold below 200 eI in new sensor modification with enlarged transistors

✧ for $2 \times 10^{15}$ $n_{eq}/cm^2$:
  ✧ monotonic effect of efficiency with threshold
  ✧ similar improvement pattern across sectors
  ✧ reaching an efficiency >90%

✧ no strong dependence on substrate voltage in range 6-15 V
... while waiting for SPS restart ... test beam at Diamond Light Source facility (UK):

- 8 keV x-ray beam: close to MIP energy deposition in the chip
- scanning position in 1-2 µm steps (corresponding to externally measured beam spot size)
- ... publication coming soon ...
Mini-MALTA is a prototype designed to improve rad.
hardness of the MALTA chip:

- modification of the sensors and improved transistors
  in the front end lead to **>97% efficiency after 1e15
  neq/cm²**
- publication under preparation

Looking ahead (full size chips):

- **Fourth submission**: chip delivered and assembled, testing started yesterday(!)
  - same slow control implementation as MaltaC
  - different substrate type for the wafer. *From TJ standard to Czochralski type*
  - should increase the size of the depletion region (more signal)

- Single Event Upset testing campaign in November

- submission of new chip in December 2019
  - half size MALTA with improved front-end transistors
  - MonoPix_V2: including 3 bits for pixel threshold tuning
Acknowledgement

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- Measurements leading to these results have been performed at the E3 beam-line at the electron accelerator ELSA operated by the university of Bonn in Nordhrein-Westfalen, Germany.

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- Dr. Ben Phoenix, Prof. David Parker and the operators at the MC40 cyclotron in Birmingham (UK).

BackUp
Asynchronous readout

- Propagation delay of asynchronous signals through double column bus up to 8 ns

- Total delay for half a column = pulse delay / 2 + signal delay / 2 = **12 ns** (-1.8 V p-well bias)
• Read-out on Xilinx 7-series VC707
• Implemented asynchronous oversampling of the data
  ■ 2 copies of the data (0.45)
  ■ 2 clock buffers (0.90)
  ■ 2 samplings per clock (0.180)
  ■ 8 samples per signal
  ■ 320 MHz clock domain
  ■ 4 GHz effective sampling
  ■ 3 to 4 samples per pulse

Xilinx application note XAPP523
Cluster size plots

Unirradiated (W6R6, S4)

Decreasing threshold, from ~600 e\(^{-}\) to ~250(unirr)/350(irr) e\(^{-}\)

Irradiated 5x10\(^{14}\) n\(_{eq}\)/cm\(^{2}\) (W6R21, S4)

Couldn't reach lower threshold
Efficiency: versus sub start voltage

W1R3 (2×10^{15} neq/cm^2)
- Large trans.
- Large trans. + extra p-well
- Large trans. + n-gap
- Std trans.
- Std trans. + extra p-well
- Std trans. + n-gap

Thr. = 160e
Thr. = 290e

W2R1 (1×10^{15} neq/cm^2)
- Large trans.
- Large trans. + extra p-well
- Large trans. + n-gap
- Std trans.
- Std trans. + extra p-well
- Std trans. + n-gap

Thr. = 155e
Thr. = 300e

W5R3 (2×10^{15} neq/cm^2)
- Large trans.
- Large trans. + extra p-well
- Large trans. + n-gap
- Std trans.
- Std trans. + extra p-well
- Std trans. + n-gap

Thr. = 120e
Thr. = 225e
Efficiency: $2 \times 10^{15} \text{ neq/cm}^2$

W5R3@SUB=10V ($2 \times 10^{15} \text{ neq/cm}^2$)

- Thr. = 120e
- Thr. = 230e

Thr. = 150e
Thr. = 130e

Thr. = 280e
Thr. = 240e