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# External scrubber implementation for the ALICE ITS Readout Unit

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Abstract

Commercial components are used in the readout electronics of the upgraded ALICE Inner Tracking System detector, hence a system-level single event upset (SEU) mitigation strategy for the FPGAs is needed to ensure correct operation. Inclusion of a flash-based auxiliary FPGA on the Readout Unit enables fault-tolerant operation, by implementing periodic blind scrubbing to correct SEUs in the configuration memory of the main FPGA, an SRAM-based Xilinx FPGA responsible for data transfer and detector configuration. This contribution discusses the external scrubber solution on the Readout Unit, focusing on the FPGA design and software design. Test results are also presented.

## Summary

The ALICE Inner Tracking System (ITS) is currently being upgraded to prepare for LHC Run 3, which is scheduled to start in 2021. The upgraded ITS will consist of 7 layers of ALPIDE ASICs (a high granularity monolithic active pixel sensor). The ALPIDEs are organized in 192 staves, consisting of 9 to 196 ALPIDEs depending on the layer. Each stave is read out by a Readout Unit (RU) located in racks inside the ALICE magnet at around 6 m from the interaction point. In the location of the RUs, the high-energy hadron flux is expected to be about 1 kHz/cm^2 in Run 3. Thus the design of the Readout Unit and of its FPGAs is required to be radiation tolerant. The main FPGA on the RU is an SRAM-based Xilinx Kintex Ultrascale FPGA, and single event upsets (SEUs) will happen in the configuration memory of the device. Scrubbing of this memory is implemented to correct the SEUs. Based on earlier irradiation campaigns with a Kintex-7 device, it was decided to use an auxiliary device (auxFPGA) to scrub the configuration memory. The auxFPGA is a flash-based Microsemi ProASIC3 A3PE600L FPGA, which is the commercial counterpart of the radiation tolerant RT ProASIC3 series. The large flash cells are radiation tolerant by technology, so mitigation is only needed on specific design elements such as registers and memory.

In order for the scrubbing to be effective, SEU mitigation techniques such as Triple Modular Redundancy (TMR) and error correction coding (ECC) is also applied to the design of the RU

main FPGA. Additionally, the design scrubbing rate is at least three orders of magnitude higher than the mean expected SEU rate. Hence, the SEUs will not accumulate, improving the effectiveness of the TMR.

Configuration and scrubbing of the main FPGA are the main tasks of the auxFPGA, utilizing the Xilinx selectMap interface. The scrubbing and configuration files are stored on a Samsung flash-memory with 1048/1024 bit hamming coding for single bit error correction and double bit error detection. The combination of ECC encoded configuration files and local TMR of the auxFPGA design achieves a high degree of radiation tolerance.

To test the functionality of the auxFPGA, a Python-based suite of unit-tests is set up and runs on the CRU host computer, which significantly shortens the testing time during development. The tests are also a reference for extended integration-tests and system level operations, as well as final detector control system functions.

The auxFPGA is currently under commissioning and integration tests are ongoing. All basic functionality works as intended, and it has been verified that continuous blind scrubbing does not interfere with the normal operation of the RU and main FPGA in normal environmental conditions. It will be shown that control, monitoring and data readout run as normal while scrubbing is continuously executed.

This contribution will give details of the design, implementation and testing in the system of the external scrubber, of the storage and management of the configuration files and of the fault injection features.

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