Design of a radiation hardened TDC with a resolution of 4 ps and an improved interpolation technique

B. Van Bockel[1], J. Prinzie[1], P. Leroux[1]

[1]KU Leuven, Dept. of Electrical Engineering (ESAT), Advanced Integrated Sensing Lab (AdvISe)

ABSTRACT

The design of a radiation hardened TDC is presented with a simulated resolution of 4 ps. This small resolution is achieved by using a novel interpolation technique that reduces the nonlinearity error of the delay line. The TDC uses a Delay Locked Loop (DLL) to compensate for resolution drift due to Total ionizing dose (TID) effects. The TDC is designed in a 65 nm CMOS Technology, using Encloses layout transistors (ELTs).

The delay line

The DLL locks the total delay of the delay line to the period of the input reference clock. This means that drifts of the individual delay elements (DEs) due to Process, Voltage, Temperature (PVT) and ionizing radiation will be compensated. The delay line consists out of 64 pseudo differential delay elements, shown in figure 1a.

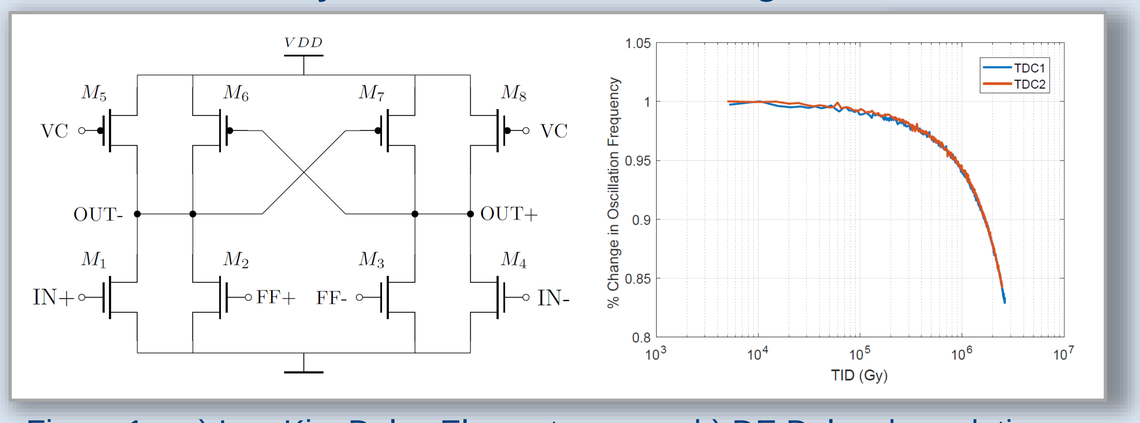

Figure 1 : a) Lee-Kim Delay Element b) DE Delay degradation

The delay line is adjustable to operate over a broad range, from 512 ps up to 1152 ps, necessary to cover all corners and to compensate for TID degradation. A reference period of 1 ns was chosen. The DE was irradiated with X-rays. Figure 1b shows the gate delay in terms of TID degradation. At 1 MGy, the gate delay degrades with only 6 %, and is easily compensated by the DLL. Additionally, the resolution of the TDC is can be tuned to match a specified resolution by switching the locations in the delay line where the DLL clock is extracted and locked to. The selection was done with a multiplexer.

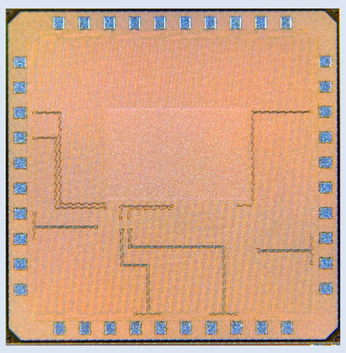

Figure 2 : Chip photomicrograph of the implemented Time- to Digital converter

Die size: 2mm x 2mm
Active area: 730 µm x 860 µm
Technology: 65 nm

Interpolation technique

To reduce the delays beyond the minimum gate delay of the technology, passive interpolation was used. The proposed technique increases the resolution of the TDC significantly and simultaneously improves the linearity of the delay line. With traditional interpolation, interpolation resistors are added between consecutive delay stages. The number of interpolations equals the amount of resistors needed to create the different phases. The bigger the interpolation the larger the mismatch between the different phases resulting in a bigger INL. This has to do with the chain of resistors. When using equal resistors the output phases are not, because every output phase sees a different resistive load. To solve this effect a detailed tuning of the individual interpolation resistor can be done, This is rather time consuming and relies on the parasitic extracted models of the layout of the DE. Therefore, In this design, an interlocked interpolation is proposed where the buffers are interpolated four times with equal resistors. With this interlocked interpolation, there are two buffer chains. Both are interpolated four times and connected to the same resistors but shifted by two resistors, thus interlocked every two phases as shown in figure 3. With this technique there is no need for tuning the resistors to match an equal phase delay because every two resistor the net is driven by a delay buffer, therefore reducing the loading effect of the resisters to each other. The mayor trade off's made by using this design is area and power for a smaller INL.

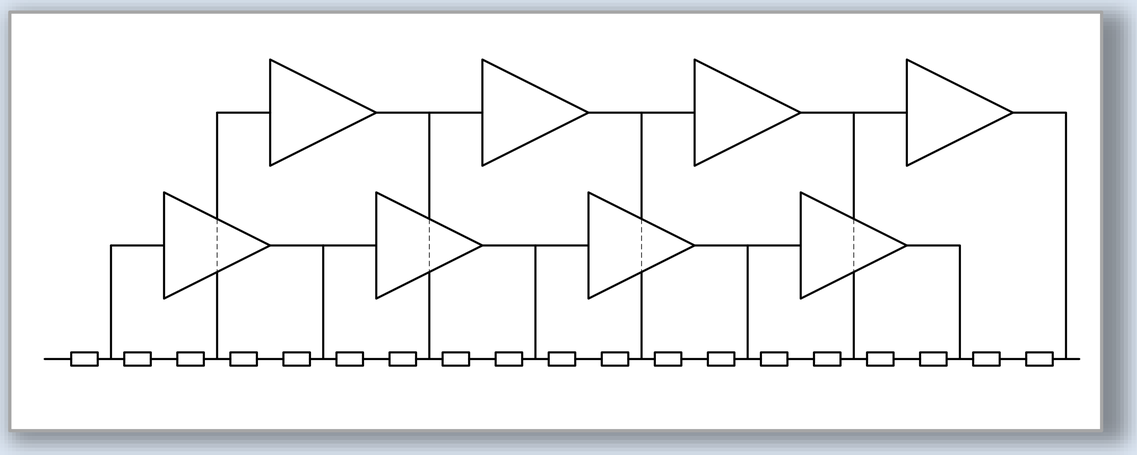

Figure 3 : Interlocked interpolation

Measurement approach

To measure the performance characteristics of the TDC, random time delays between the reference clock and the start and stop channel will be injected. The outputs taken from every measurement will be combined in a histogram of which the INL error can be read from.

Conclusion

The presented TDC has a promising single shot resolution of 4 ps, and can be applied for high energy physics applications. X-ray experiments have proven that the TDC can operate up to a dose of at least 1 MGy. The new interlocked interpolation technique improves the linearity of the TDC by 45%.